Fakultät für Elektrotechnik und Informationstechnik
Arbeitsgebiet Bordsysteme

technische universität dortmund

Report

Impact of Lowering the HBM-IC-Robustness on the Automotive-System-Level-Robustness

to

ESD Forum e.V.

19th September 2011

Dipl.-Ing. Friedrich zur Nieden
Dipl.-Ing. Stanislav Scheier
Prof. Dr.-Ing. Stephan Frei

Arbeitsgebiet Bordsysteme
Technische Universität Dortmund
Friedrich-Wöhler-Weg 4
D-44227 Dortmund

Contents

Introduction

The impact of a lower HBM-IC-robustness on the ESD-robustness of automotive systems is currently discussed in industry. In a whitepaper an industry council of semiconductor manufacturers proposes the lowering of component level HBM / MM ESD specifications to save costs [1]. The proposal is based on the following considerations:

- Sufficient protection for packaging and handling is provided by 1 kV HBM testing
- Statistics show that there is no impact of different IC HBM-ESD robustness levels on the ESD failure rates
- Only new ICs applied to circuits without direct connection to automotive electronic control unit connectors would be affected
- Function levels of ICs remain the same but the ESD-robustness is lowered

As a reaction to the proposal the DKE working group AK 767.13.5 proposes detailed investigation on the topics due to the following reasons [2]:

- A lowering of the IC robustness might affect the systems' ESD robustness in case of coupled ESD between global[1] and local pins
- Critical pulse energies at IC pins caused by ESD coupling from connector pins depend on the PCB layout
- If the OEM ESD specifications remain the same, how does a lowering of HBM levels affect the IEC testing?
- What effects can be observed with cable discharge events at connector pins?
- Is there any effect on the choice of external ESD protection elements?

The main objectives of the investigation are based on the questions discussed among members of the automotive industry concerning the publications by the industry council:

- Estimation of the impact of ICs with lower robustness on automotive systems
- Quantification of the disturbances by on-PCB cross-talk
- Quantification of the disturbances through connected cables
- Specification of external ESD protection strategies for compliance with Packaging and Handling demands

[1] IC pins can be separated in local and global pins. Global pins can be connected to the ECU connector and might be threatened directly by ESD currents. Local pins have no direct connection to the ECU connector.

The research work is based mainly on measurements and simulations. All simulations methods are verified by measurements. A demonstrator PCB was developed considering typical automotive electronic configurations. Different test pulses were applied to investigate coupling effects between transmission lines and estimate the disturbance potential for ICs. Common automotive ICs were used as realistic victims (µC, LIN, CAN) and failure levels with direct or field coupled currents were identified by measurement. In this context the effectiveness of external ESD protection elements has been lined out. Another special aspect dealt with the possible disturbance by trace loops on PCBs. Simple loop configurations were considered in the design of the demonstrator.

As a second step models of all components on the demonstrator PCB and in the environment are provided. Transmission line models are used to describe on-PCB traces and cables. The models of conductors were verified by measurement. Coupling of multi conductor transmission line models was verified using 3D simulation.

µC, LIN and CAN pins, which are selected as victims for ESD pulses on the demonstrator, are characterized and failure models were developed. The required characteristic datasets were measured using special developed PCBs for the application of TLP (transmission line pulser).

Models of different testing devices like HBM- and IEC generators were applied to investigate the discussed questions. The interconnection of all component models allowed the simulation of maximum coupled amplitudes and energies on IC and connector pins.

The impact of different HBM failure levels on the robustness of automotive electronic control units has been considered by a modification of the parameters of the IC ESD failure models.

1 Demonstrator PCB and PCBs for IC characterization

The objectives defined in introduction are investigated by simulation and measurement. For measurement a testboard was designed considering critical PCB-trace configurations. Different types of automotive IC pins can be selected as terminations. The testboard concept, considering LIN-, CAN-transceivers and an 8-bit µC, is described in detail in section 1.1.

In order to create IC failure models, different characteristic datasets of each IC pin have to be measured with a TLP setup for modeling. To ensure a high level of accuracy two special PCBs were designed. The layout for LIN and CAN-transceivers is shown in section 1.2. Selected pins of an 8-bit µC are characterized using the second board described in the same section.

All PCBs are designed double-sided and were manufactured on FR4 material (thickness: 1.55 mm). The thickness of the copper traces is 35 µm.

1.1 ESD demonstrator PCB

The demonstrator PCB is designed to investigate the disturbance of automotive systems by on-PCB coupling effects caused by ESD. As a second item the potential failure of ICs with lower ESD robustness is analyzed. The allover layout is shown in Figure 1. It can be divided into 4 main sections:

- Voltage regulator
- Cross-talk section with long parallel traces
- Section for investigations with µC (XC-864)
- Section for investigations with LIN transceivers
- Section for investigations with CAN transceivers

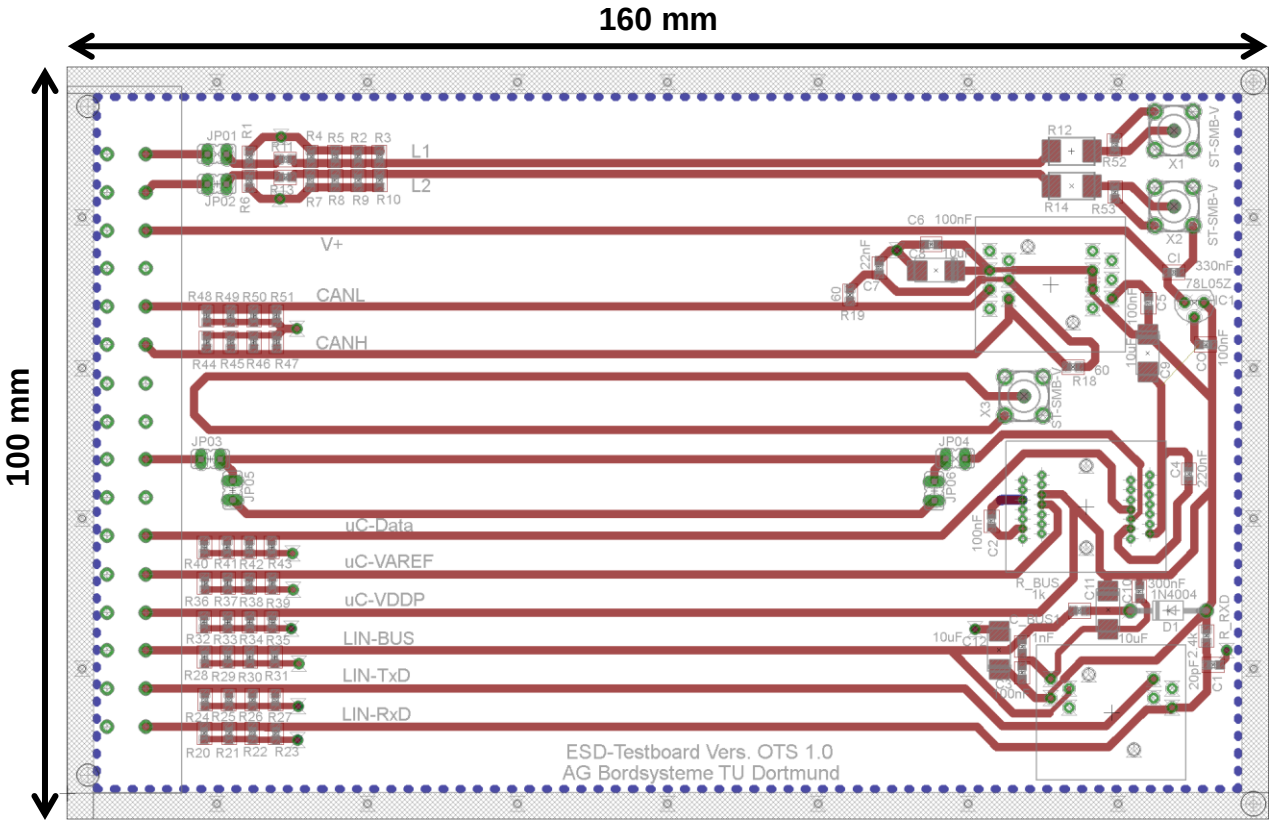

Figure 1: ESD demonstrator PCB layout

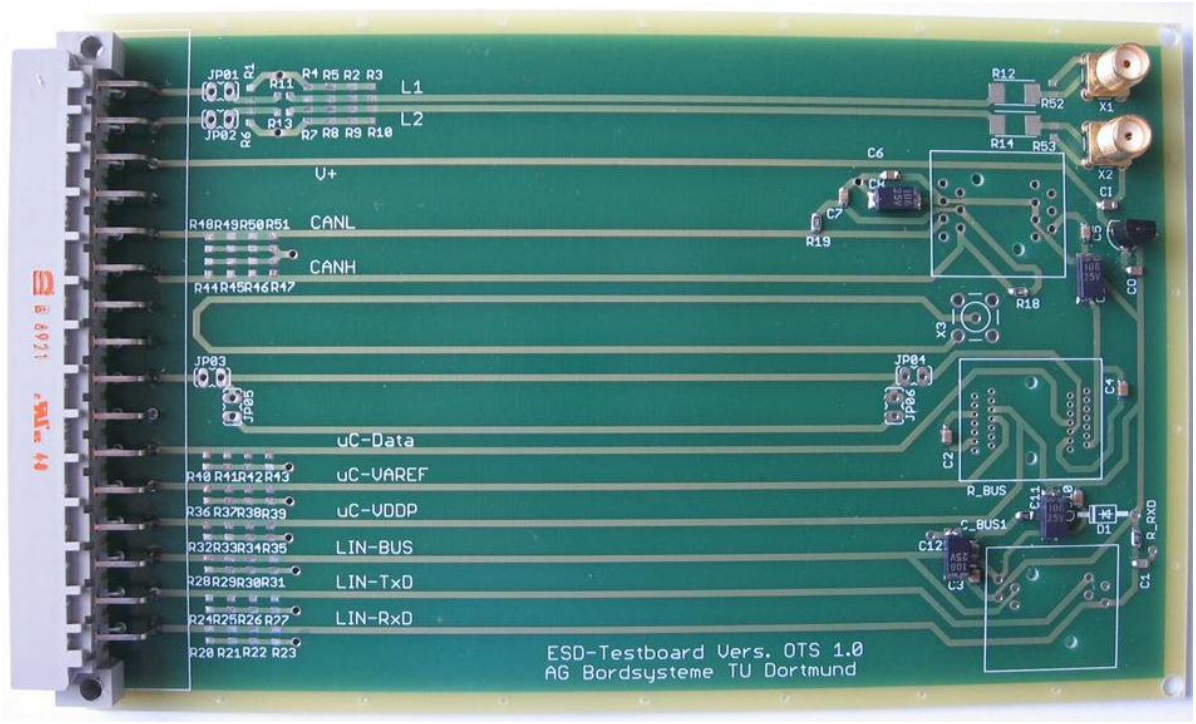

Figure 2: ESD demonstrator PCB with connector

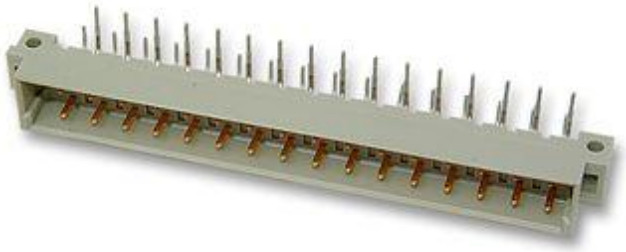

Figure 3: Connector of demonstrator

A 2-row “Harting 09 04 132 6921” connector with 32 pins was chosen for the demonstrator. It is similar to typical automotive connectors. The allover width is 88.9 mm. The connector is suitable for a 5.08 mm grid.

1.1.1 Voltage regulator

A “Texas Instruments LP2950” voltage regulator was considered in the layout to provide a 5 V supply to the ICs, if powered tests are required. The functional block diagram is shown in Figure 4. Basic characteristics of the element are listed below:

- Wide input voltage range: up to 30 V
- Stable with low ESR (>12 mΩ) capacitors
- Rated output current of 100 mA
- Current- and thermal-limiting features
- Low dropout: 380 mV (typ.) at 100 mA
- Low quiescent current: 75 µA (typ.)

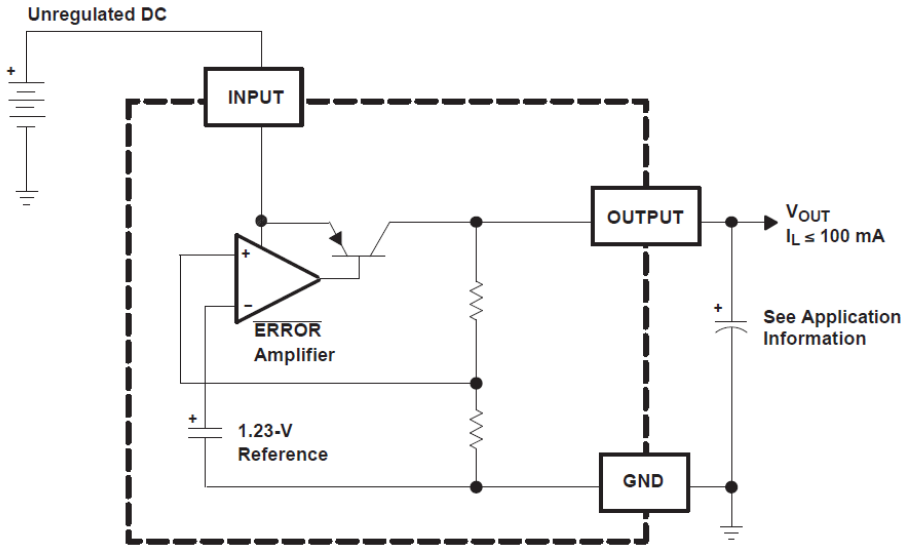

Figure 4: Functional block diagram of voltage regulator

In the layout the voltage regulator is connected to a 330 nF and 100 nF capacitor on the input and output pins (Figure 5). Larger blocking capacitors are not used as influence on ESD pulse propagation is low.

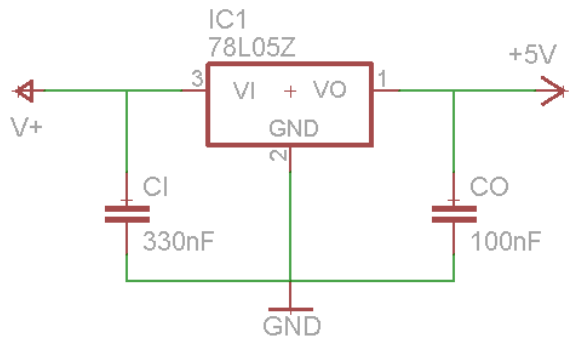

Figure 5: Circuit of voltage regulator

1.1.2 Coupling between parallel PCB traces

Basic coupling effects can be investigated by two parallel PCB traces. The layout of the coupling (cross-talk) section is shown in Figure 6. A charged structure can be discharged into the upper conductor and the coupled signal can be measured on the lower conductor. Two traces of 1 mm width are placed in 0.5 mm distance to each other. Each trace can be terminated by several serial and parallel elements at both ends. Jumpers allow including the connector in the setup if additional loads or wires should be connected or the influence of the connector should be part of the investigation. The signals on both lines can be measured with an oscilloscope via SMA-connectors or by using small current sensors like Tektronix CT1 or CT6.

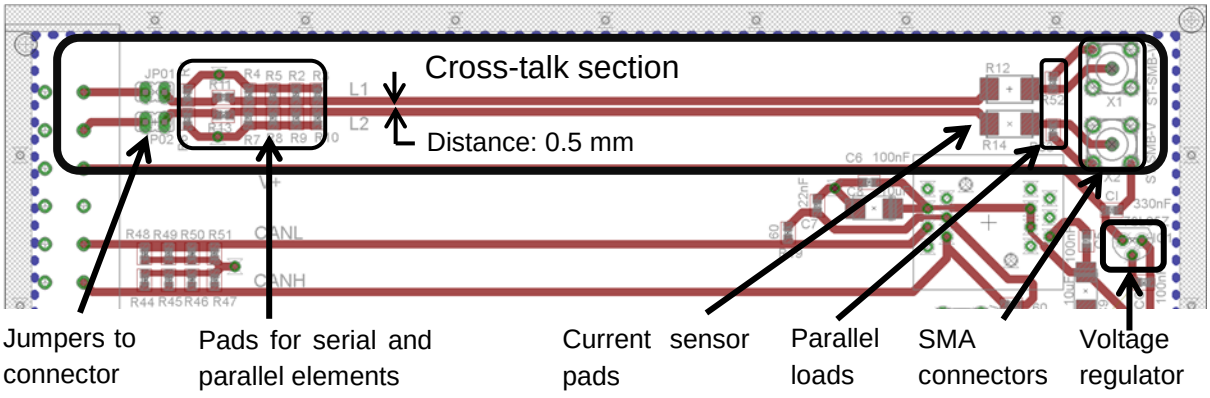

Figure 6: Cross-talk section of demonstrator

Field coupling on PCBs can occur if conducting loops are part of a design. On the demonstrator board two loops were designed to investigate the potential disturbance of ICs by this effect. If a network is discharged into a conductor close to the loop the induced current can be measured via a SMA connector with an oscilloscope. A

second loop configuration can be chosen with jumpers. The discharge current can be impressed into the connector pin and the loop trace can be terminated with an IC pin.

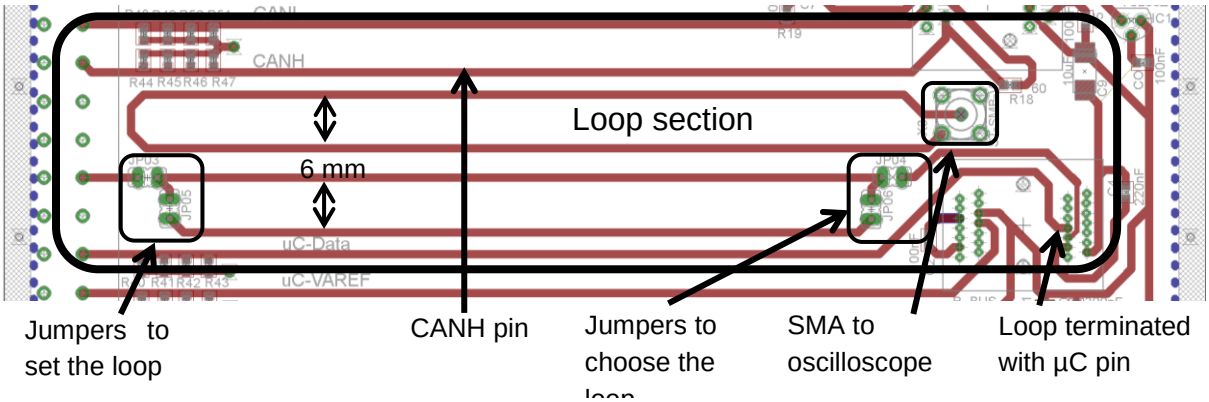

Figure 7: Coupling into loops

1.1.3 µC

The main functionality of automotive electronic control units (ECU) is implemented with programmable microcontrollers. The complex ICs contain different types of elementary circuits. To increase the variety of test options on the demonstrator board several pins of an Infineon 8-bit XC864 µC are considered in the layout. The ESD robustness according to the datasheet is specified up to a testing level of 2 kV HBM for all pins.

IC	Pins	ESD protection level
Infineon XC864 8-bit µC TSSOP-20	All pins	HBM -2kV..2kV C=100pF R=1,5 kOhm CDM -500V..500V C=330pF R=150 Ohm

Table 1: ESD protection levels of µC pins as specified in datasheet

Two multipurpose I/O pins and two supply pins (“I/O port supply”, “core supply monitor”) were selected for testing. The configuration is shown in Figure 8. Although the ESD specification is similar for all pins, a different behavior is expected during characterization and testing.

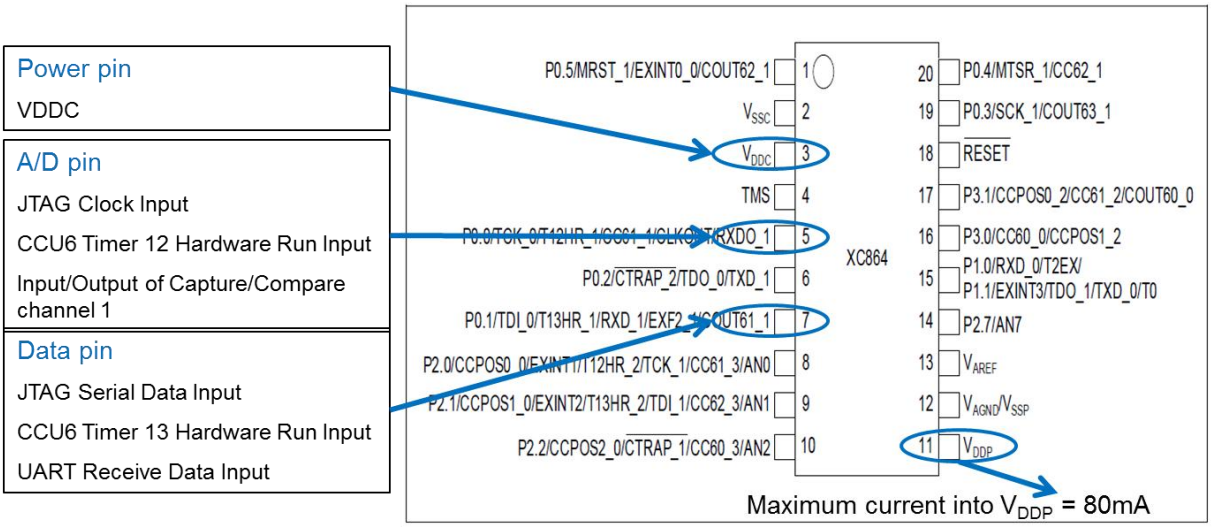

Figure 8: Selected pins of µC for investigation on demonstrator PCB

In the circuit diagram in Figure 9 all connections to the µC-IC are drawn. A 10 µF and a 300 nF capacitor are connected at VDDP pin. 100 nF are connected to reset input and 220 nF are soldered between VDDC and supply ground pins.

The layout of the demonstrator in the µC section is shown in Figure 10. Because of a better availability a TSSOP28 socket is used in the design so that 8 pins of the socket are left open on the IC side. The data pin, VREF pin, VDDP pin and AD pin are connected to the connector and can be tested with different testing devices. In case of VDDP, VAREF and Data input ESD protection elements can be added parallel to ground.

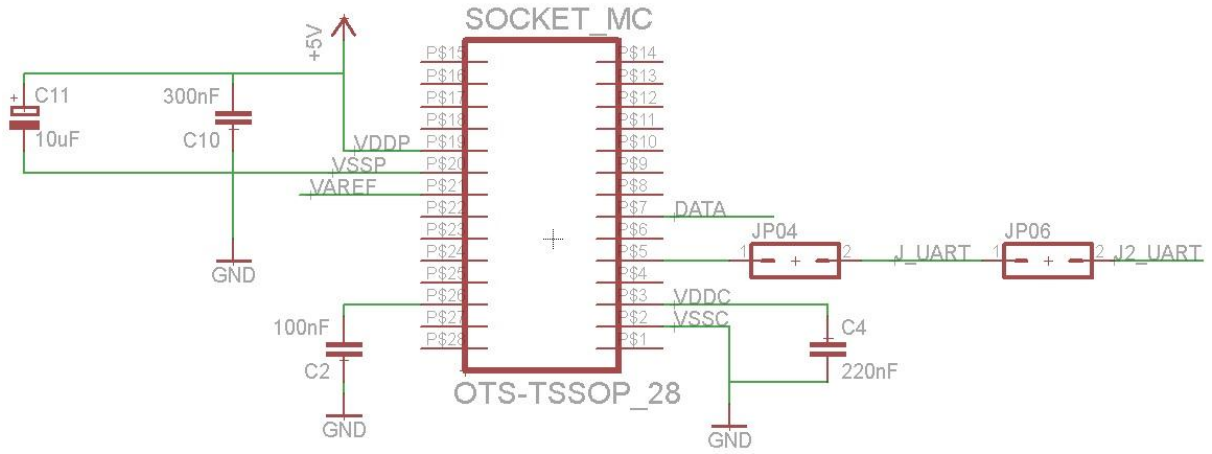

Figure 9: Circuit connected to µC on demonstrator

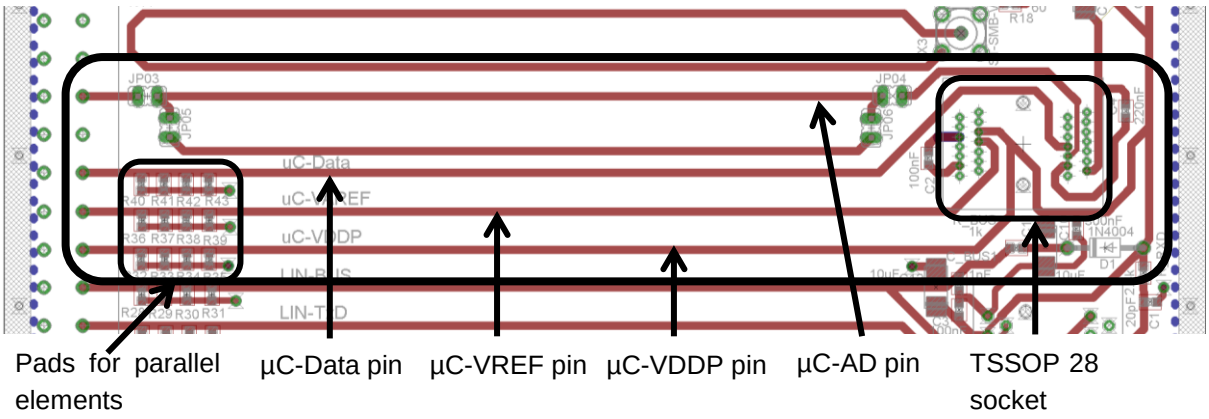

Figure 10: µC section on demonstrator PCB

1.1.4 LIN transceivers

Three different LIN transceivers were selected for testing. In comparison to microcontrollers a higher level of ESD protection is specified for most pins. Available parameters from Datasheet are listed in Table 2.

IC	Pins	ESD protection level
Infineon TLE7259-2GE LIN Transceiver PG-DSO-8	Bus Pins	IEC -11kV ..11kV C=150pF R=330 Ohm IEC61000-4-2
	Vs, Bus, WK vs. GND	HBM -6kV..6kV C=100pF R=1,5 kOhm
	All pins	HBM -2kV..2kV C=100pF R=1,5 kOhm
Atmel ATA6662C LIN Transceiver SO8	Vs, LIN vs. GND WK	IEC -6kV ..6kV C=150pF R=330 Ohm IEC61000-4-2 IEC -5kV ..5kV C=150pF R=330 Ohm IEC61000-4-2
	Vs, LIN, WK, INH Pins vs. GND	HBM -6kV..6kV C=100pF R=1,5 kOhm
	All other Pins	HBM -3kV ..3kV C=100pF R=1,5 kOhm MM -100V ..100V C=500pF R=10 Ohm L=0.75µH CDM -750V..750V C=330pF R=150 Ohm

Table 2: ESD specifications of selected LIN transceivers

The LIN-bus, LIN-RxD and LIN-TxD pin are connected to the connector on the demonstrator board. For protection parallel elements can be soldered in the current path of each pin. ESD-tests should be done with 100 nF capacitors at LIN-RxD and LIN-Bus pins. The circuit and layout section for LIN transceivers is shown in Figure 11 and Figure 12.

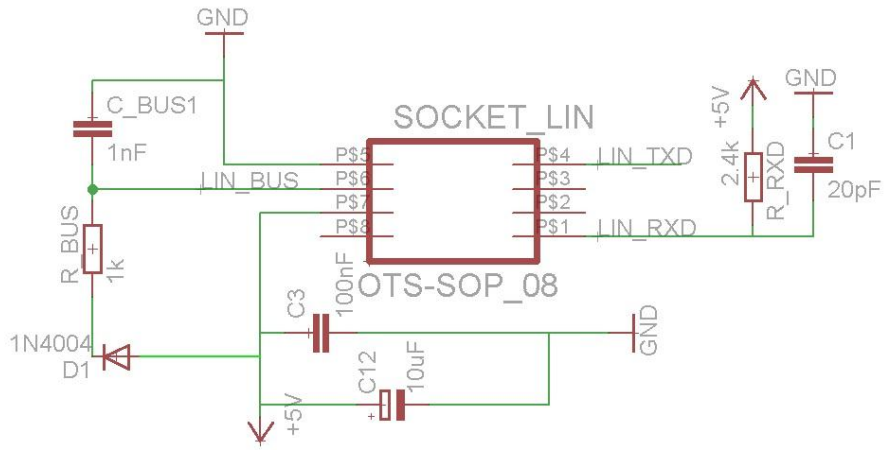

Figure 11: Circuit for LIN transceivers on demonstrator PCB

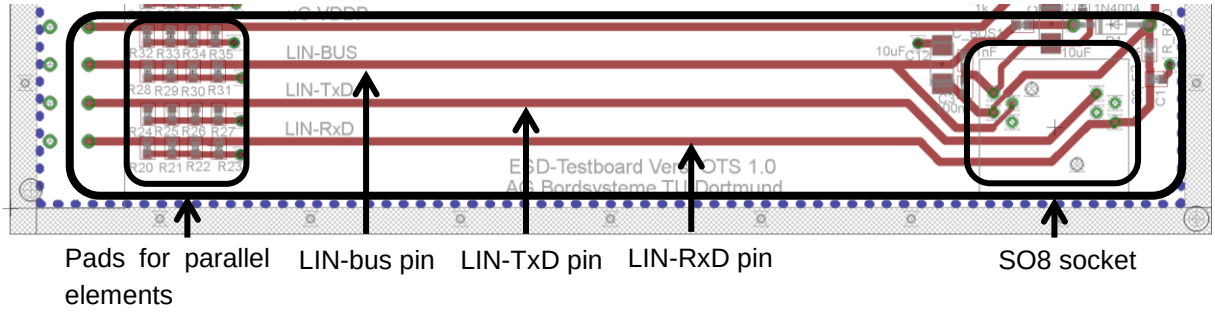

Figure 12: LIN section on demonstrator PCB

1.1.5 CAN transceivers

Similar to LIN transceivers often CAN transceivers are part of automotive electronic control units. The selected ICs are designed to withstand minimum 6 kV IEC discharge for global pins. According to Table 3 local pins are specified with 2 kV HBM except the SPLIT-pin of the TLE 6251 G transceiver. The layout is shown in Figure 14. The CANH- and CANL-pins are connected to the demonstrator connector and can be tested in different configurations with optional parallel elements. For ESD testing SPLIT termination and 100 nF at V_{cc}, $V_{\mu C}$ and V_s pins can be also considered as can be seen in the circuit diagram in Figure 13.

IC	Pins	ESD protection level
Infineon TLE 6251 G HS-CAN Transceiver P-DSO-14-13	CANH, CANL	IEC -6 kV ..6 kV C=150 pF R=330 Ohm IEC61000-4-2
	CANH, CANL, WK	HBM -6 kV..6 kV C=100 pF R=1,5 kOhm
	SPLIT	HBM -1 kV..1 kV C=100 pF R=1,5 kOhm
	All other pins	HBM -2 kV..2 kV C=100 pF R=1,5 kOhm
NXP TJA1041T SO14	CANH, CANL, SPLIT	HBM -6 kV ..6 kV C=100 pF R=1,5 kOhm
	TXD, RXD, VI/O, STB	HBM -3 kV..3 kV C=100 pF R=1,5 kOhm
	All other pins	HBM -4 kV..4 kV C=100 pF R=1,5 kOhm
	All pins	MM -200 V..200 V C=200 pF R=10 Ohm

Table 3: ESD specifications of selected CAN transceivers

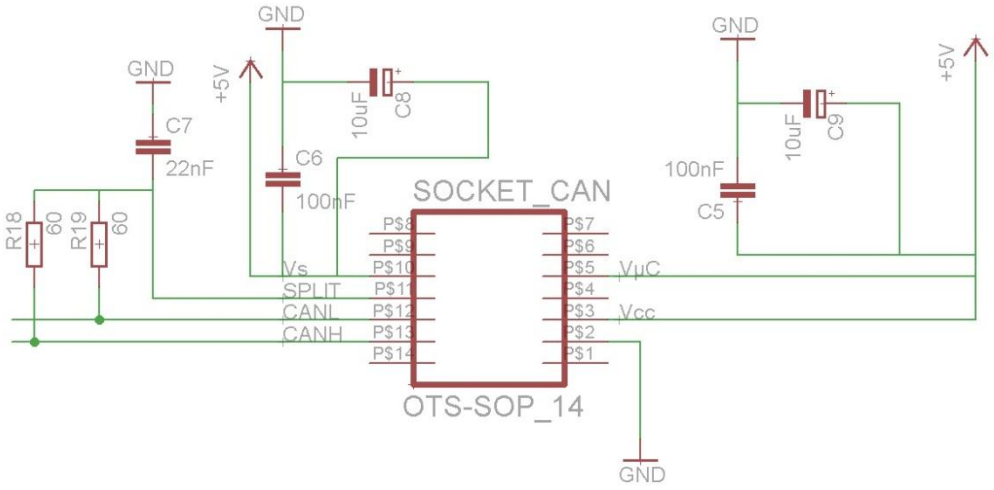

Figure 13: Circuit for CAN transceivers on demonstrator PCB

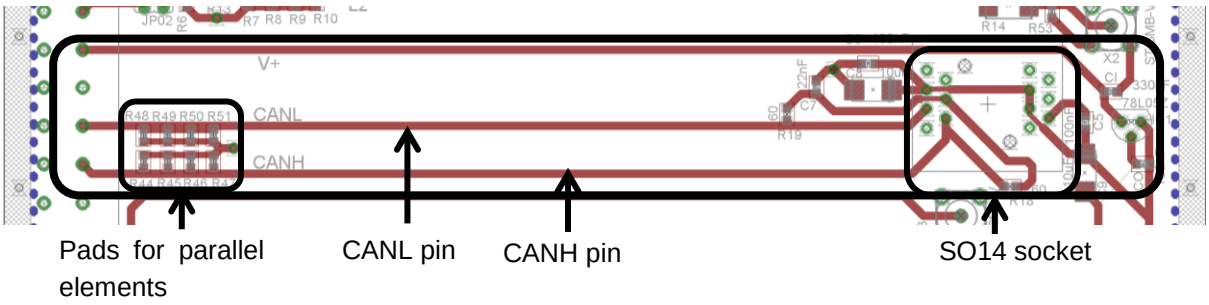

Figure 14: CAN section on demonstrator PCB

1.2 TLP-testboards for µC, LIN- and CAN-transceivers

The impact of ICs with lower ESD robustness is partly investigated by simulation techniques. A detailed TLP (transmission line pulser) characterization of all selected

IC pins is required for modeling. For measurement with the TLP the ICs are placed on special testboards. The layout is optimized for short lengths of PCB traces. To prevent reflections due to mismatch, traces are designed to have a line impedance of 50 Ω in order to match to the 50 Ω source impedance of the TLP. The PCBs with dimensions 60 mm x 80 mm are shown in Figure 15 and Figure 16.

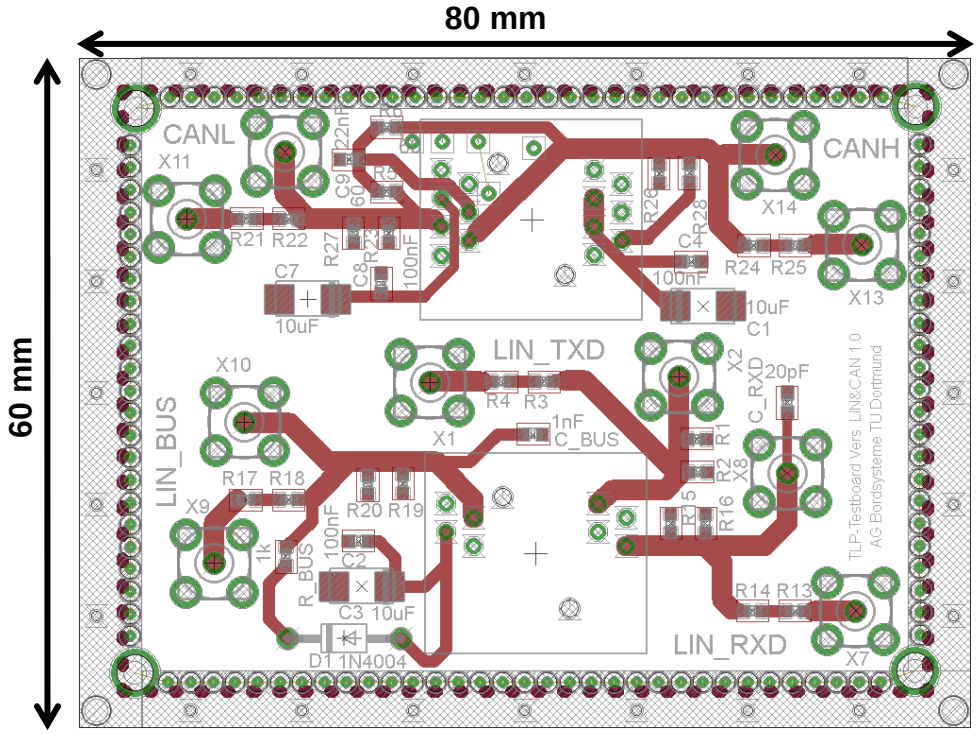

Figure 15: TLP testboard with sockets for LIN and CAN transceivers

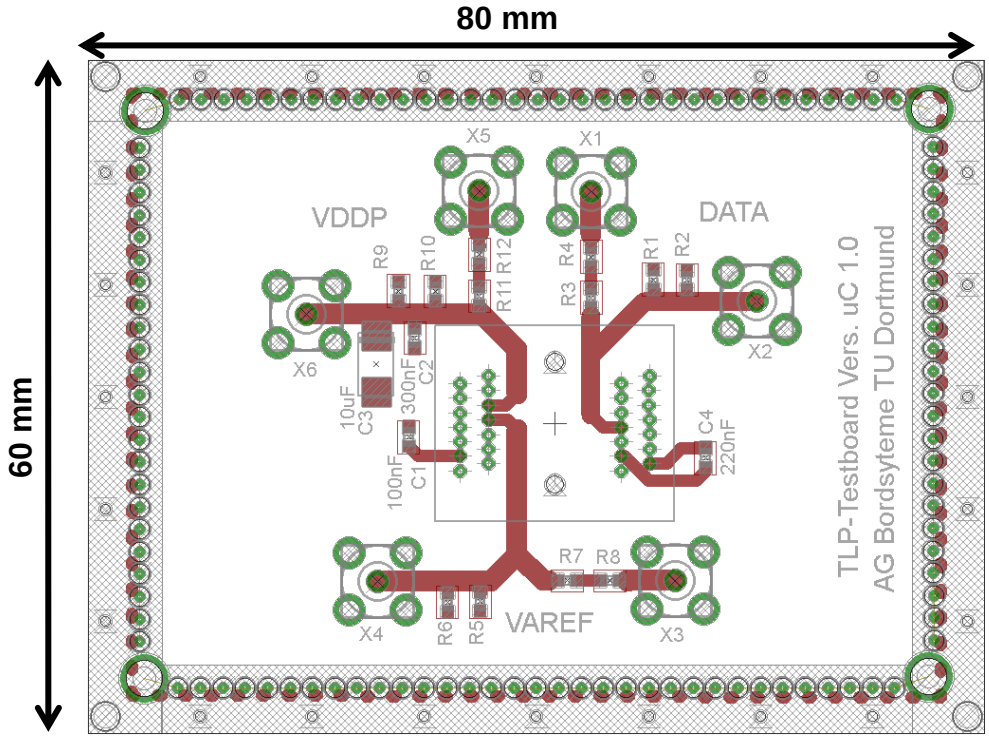

Figure 16: TLP testboard with µC socket

Capacitors of 10 µF can be soldered parallel to the voltage supply pins of all ICs for characterization. Similar wiring and circuits as described for the demonstrator PCB are considered in the TLP PCB layout to make sure that testing conditions are comparable in each setup. As a second testing option the ESD robustness of single IC pins protected by parallel devices can be measured with the TLP setup.

2 Modeling of components

In section 2 modeling techniques and already available and during this project created models for the simulation of the ESD pulse propagation on PCBs are described.

2.1 Pulse generators

Different standardized pulse generators are used to specify the ESD robustness of electronic systems on component and system level. The models of HBM, IEC and TLP pulse generators are described in the following sections.

2.1.1 **HBM model**

The Human Body Model (HBM) is traditionally used for basic ESD-characterization of integrated circuits. The waveform is defined e.g. in the non-automotive JEDEC JESD22-A114F standard [3]. In [4] a proposal for a HBM generator model is described. The equivalent circuit is shown in Figure 17. Differing from the literature approach the inductor L_S has been changed to 5 µH.

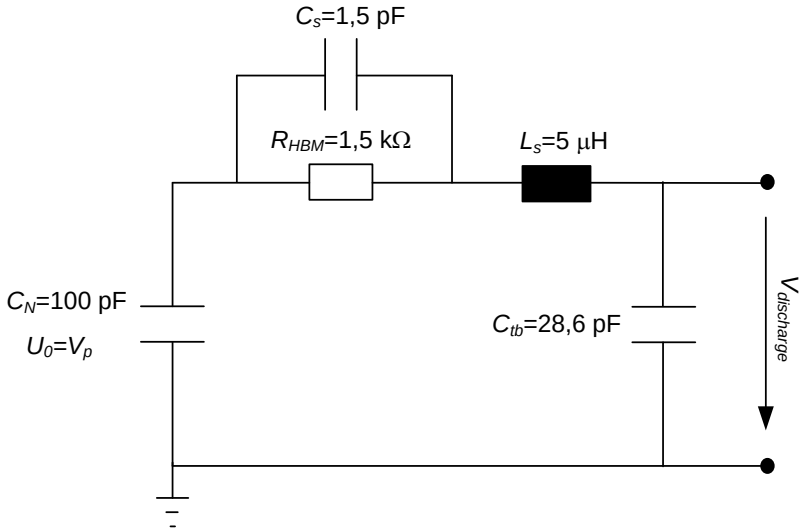

Figure 17: General equivalent circuit of basic HBM generator model

For waveform verification the currents flowing through a 500 Ω resistor and shorted circuit is measured. The simulated discharge of the HBM model through a 1 Ω resistor is shown in Figure 18.

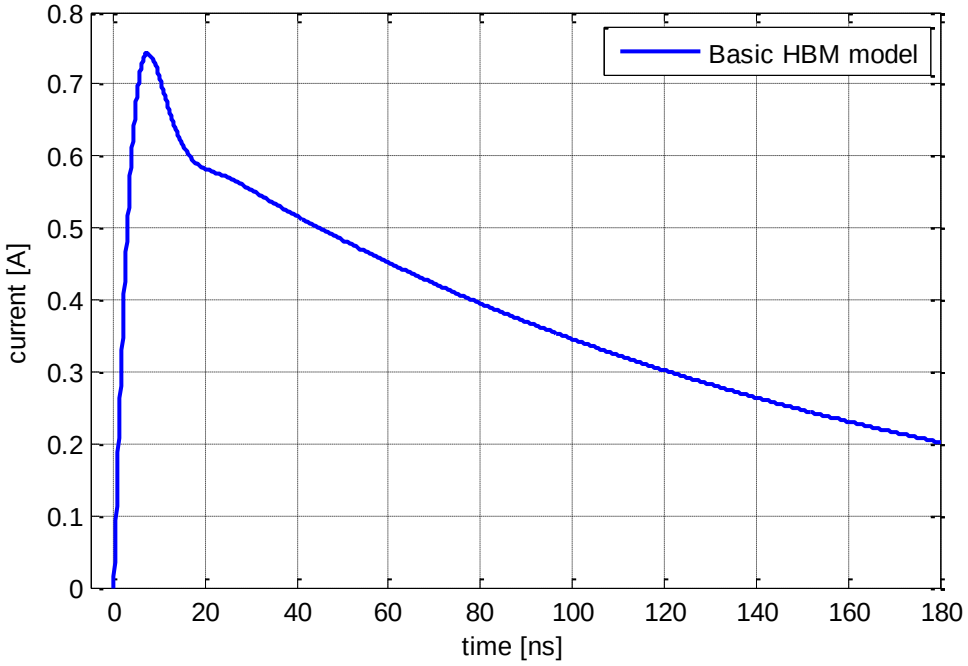

Figure 18: Discharge of basic HBM generator model with 1 Ω load and 1 kV charging voltage

For verification with the short circuit load a pulse rise time of 2-10 ns and peak amplitude of 0,6 to 0,74 A is required if the capacitor is charged with 1000 V.

According to the standard a rise time of 5-25 ns and peak current amplitude of 0,37 to 0,55 A has to be measured for the same charging voltage if the generator is connected to 500 Ω. The simulated waveform is shown in Figure 19.

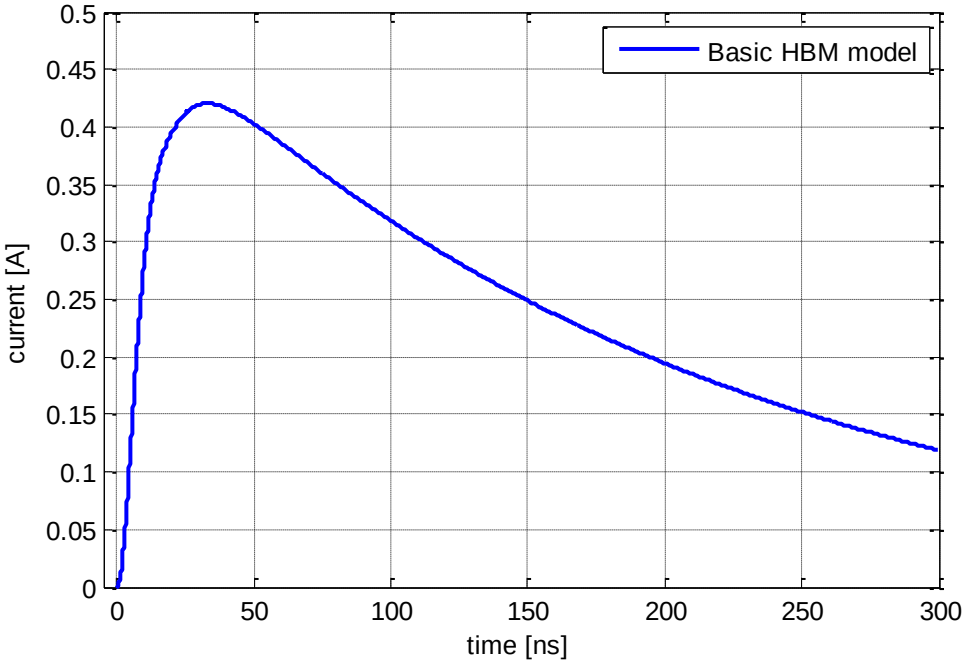

Figure 19: Discharge of basic HBM generator model with 500 Ω load and 1 kV charging voltage

2.1.2 **Basic IEC generator model**

As a general approach the current waveform which is specified in to the standard IEC 61000-4-2 can be simulated by two parallel R, L, C circuits with charged capacitors. The general equivalent circuit is shown in Figure 20. Here the standardized network elements of the ESD-generator are represented by R_1 and C_1. The inductor L_1 is considered to be the obligatory ground strap with the length of about 2 m.

Physically the first peak of the pulse is shaped by additional lumped and parasitic elements around and in the tip of the ESD-generator.

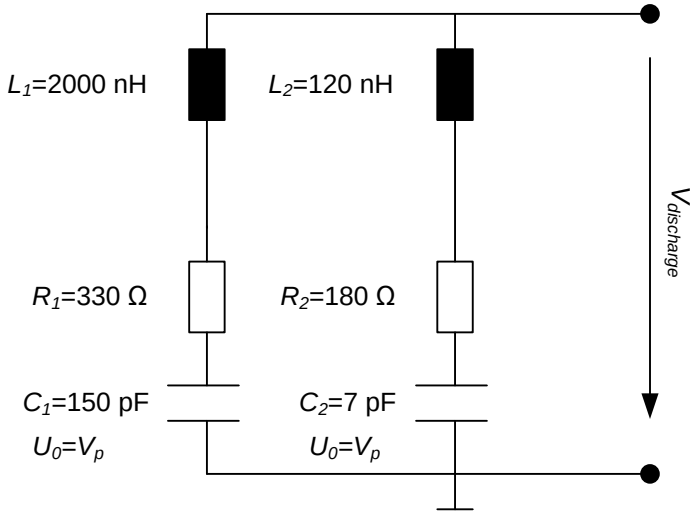

Figure 20: General equivalent circuit of basic ESD-generator model

According to the IEC 61000-4-2 standard the current waveform has to be verified with a low ohmic current sensor. The resulting current shape is shown in Figure 21. The first peak and accurate rise-time can be seen in detail in Figure 22.

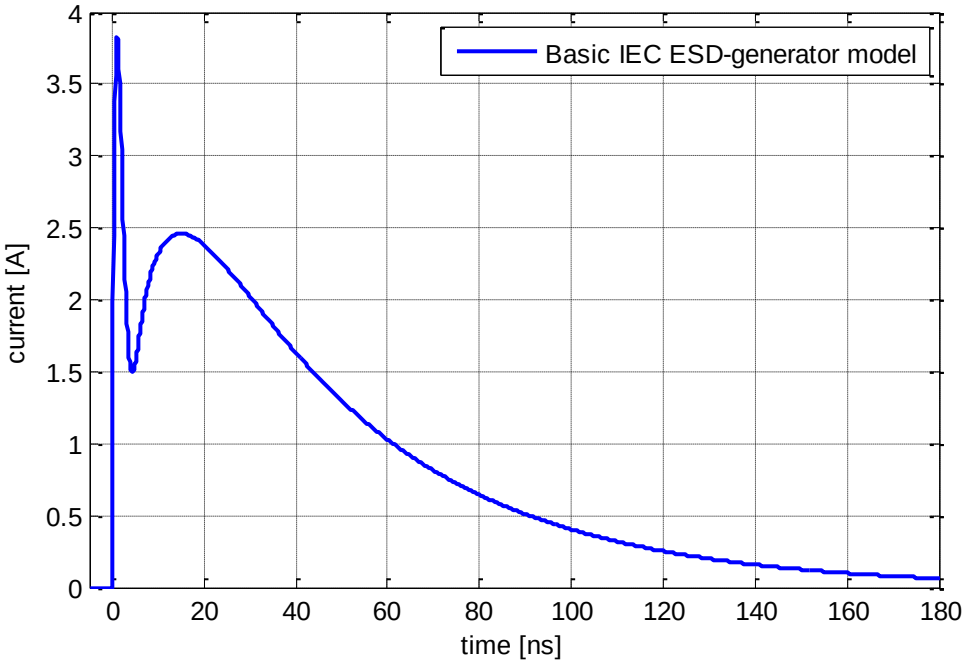

Figure 21: Discharge of basic IEC ESD-generator model at 2 Ω load with 1 kV charging voltage

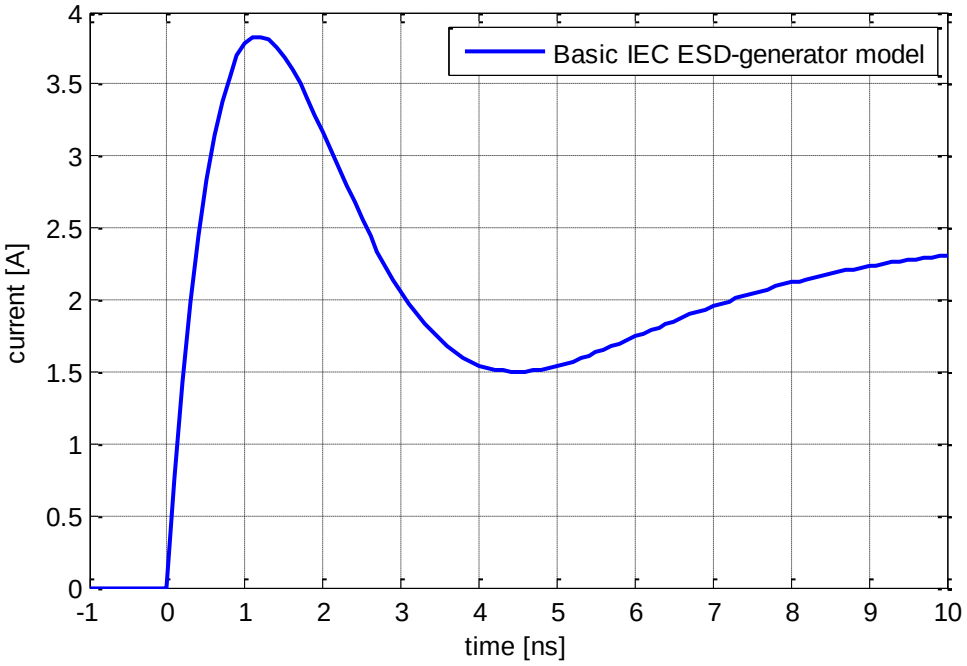

Figure 22: First peak current of basic IEC ESD-generator model at 2 Ω load with 1 kV charging voltage

2.1.3 **IEC NoiseKen model**

An advanced circuit simulating the discharge of a NoiseKen IEC generator is given in Figure 23. The model has been verified by measurement on different low and high-ohmic loads. More detailed information can be found in [5] and [6].

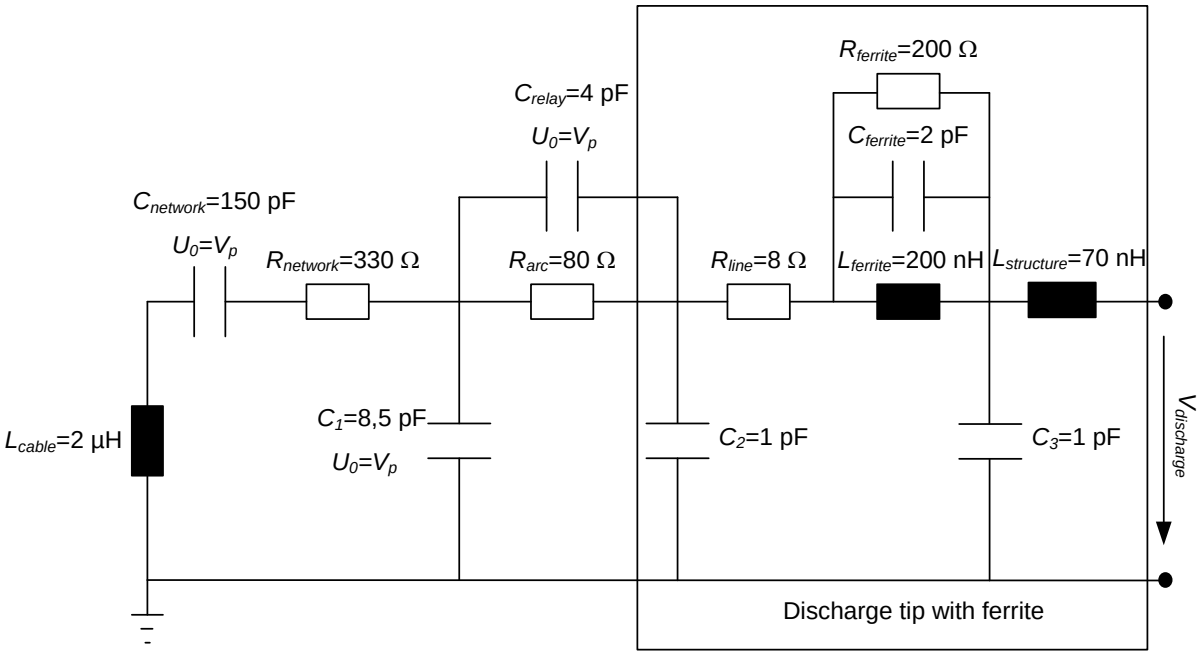

Figure 23: General equivalent circuit of NoiseKen ESD-generator

The resulting current shape is shown in Figure 24. The first peak and accurate rise-time can be seen in detail in Figure 25.

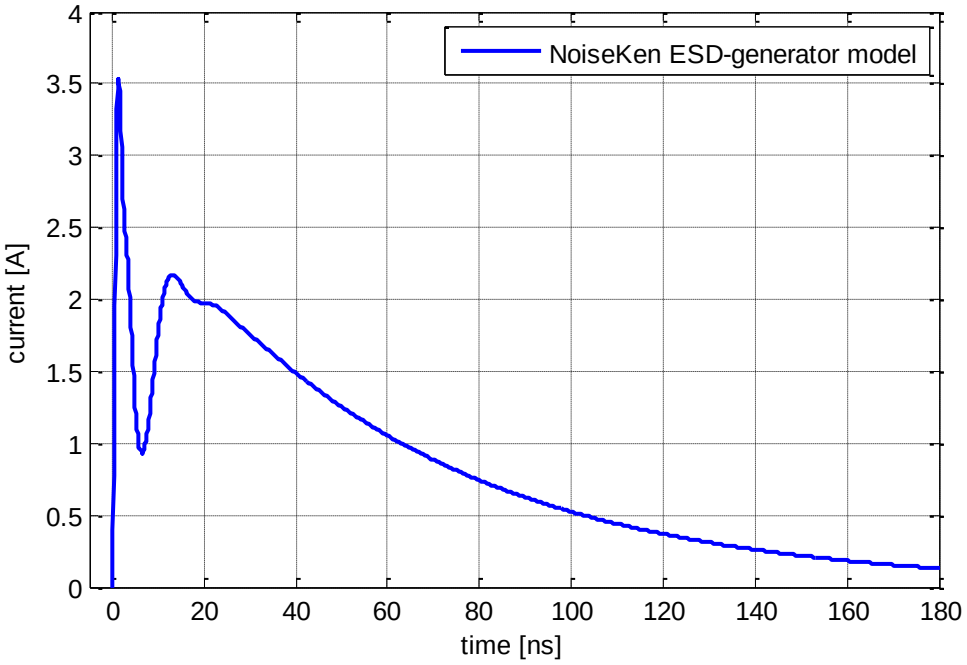

Figure 24: Discharge of NoiseKen ESD-generator model with 2 Ω load and 1 kV charging voltage

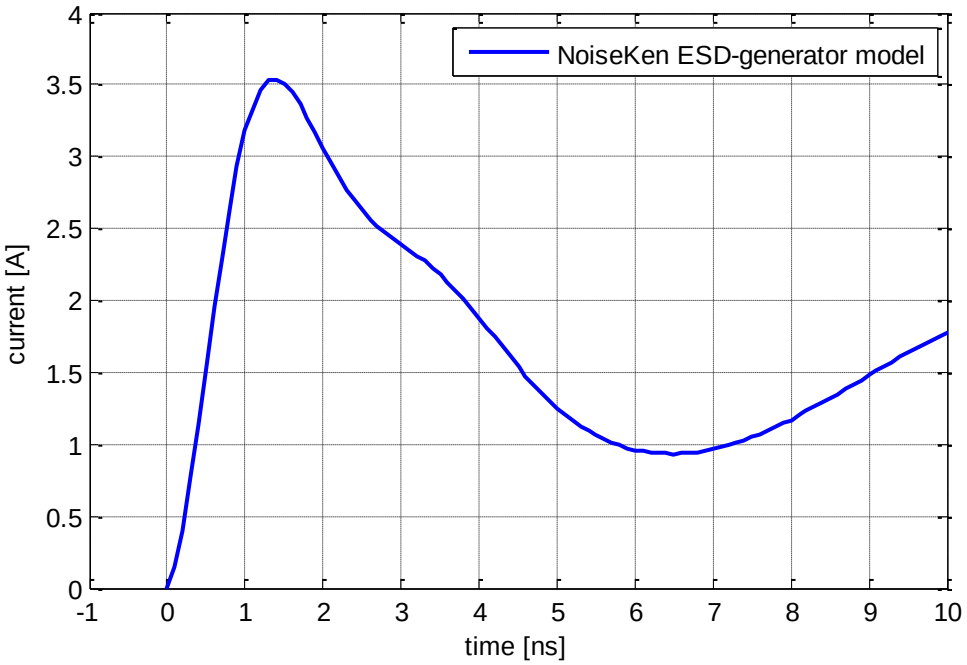

Figure 25: First peak current of NoiseKen ESD-generator model with 2 Ω load and 1 kV charging voltage

2.1.4 **TLP model**

A transmission line pulser (TLP) can be used for high power characterization of ICs. In some approaches the TLP can also be applied as testing device for ESD robustness. To achieve reliable simulation results an exact modeling of the TLP is required. In comparison to the modeling of ESD-generators, some components of the used TLP [7] can be directly mapped to model components. A part of the equivalent circuit is shown in Figure 26. The model has been verified by measurement on different low and high-ohmic loads. More information can be found in [8].

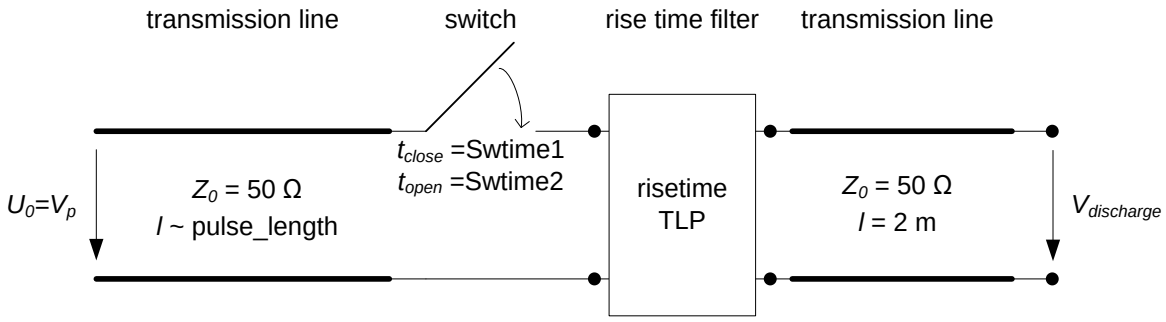

Figure 26: Diagram of TLP model

The pulse amplitude and the pulse length are mainly affected by the first transmission line. For simulation a lossless VHDL-AMS transmission line model is used, where the line charge V_p can be set as an initial condition. The pulse length is adjusted defining the length of the charged line according to the following equation:

$$length = \frac{pulse\_length}{10\ \text{ns}}$$

The wave impedance Z_0 is set to 50 Ω. The propagation velocity of the line is set to $v_0 \approx 2{,}0 \cdot 10^8$ m/s.

The line is discharged via a relay which is considered to be an ideal switch. The rising and falling edges can be controlled by the connected rise time filter. A detailed description can be found in [9]. Three different rise times (1,2 ns, 2,0 ns or 5,0 ns) are implemented.

Finally the pulse propagates through a second 50 Ω transmission line to the DUT. In this case a VHDL-AMS model including losses is used to improve the accuracy of the simulated pulse shapes.

The model impedance mainly is determined by the rise time filter and the wave impedance of the transmission lines. Simulated current and voltage shapes are shown in Figure 27 and Figure 28 for a charging voltage of 1000 V and a 1,2 ns rise time filter.

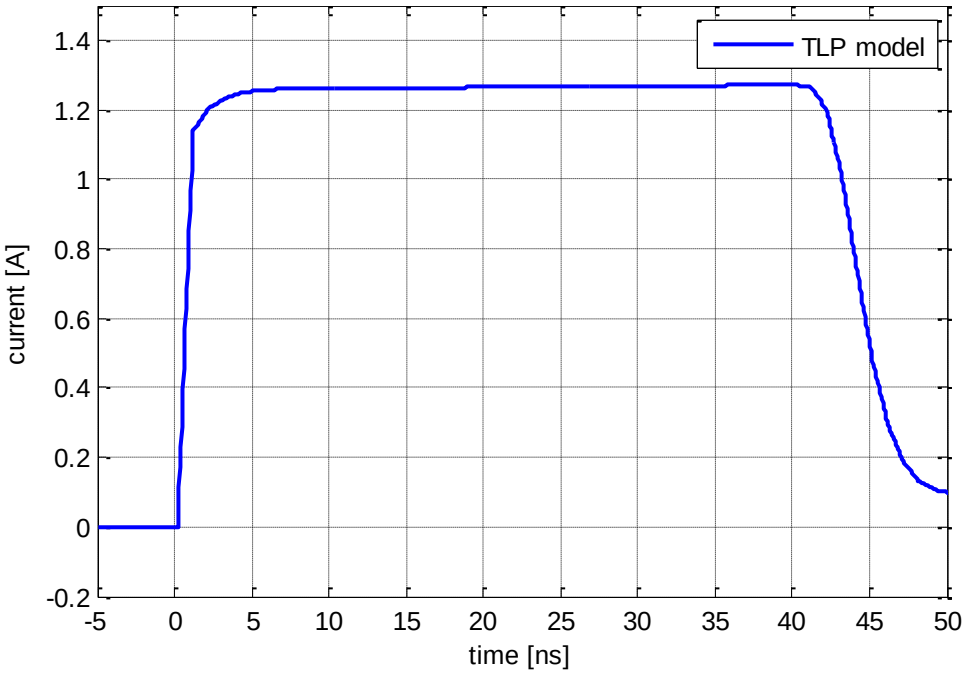

Figure 27: Simulated current of discharge of the TLP model into 50 Ω with 40 ns pulse width, 1,2 ns rise time and 1 kV charging voltage

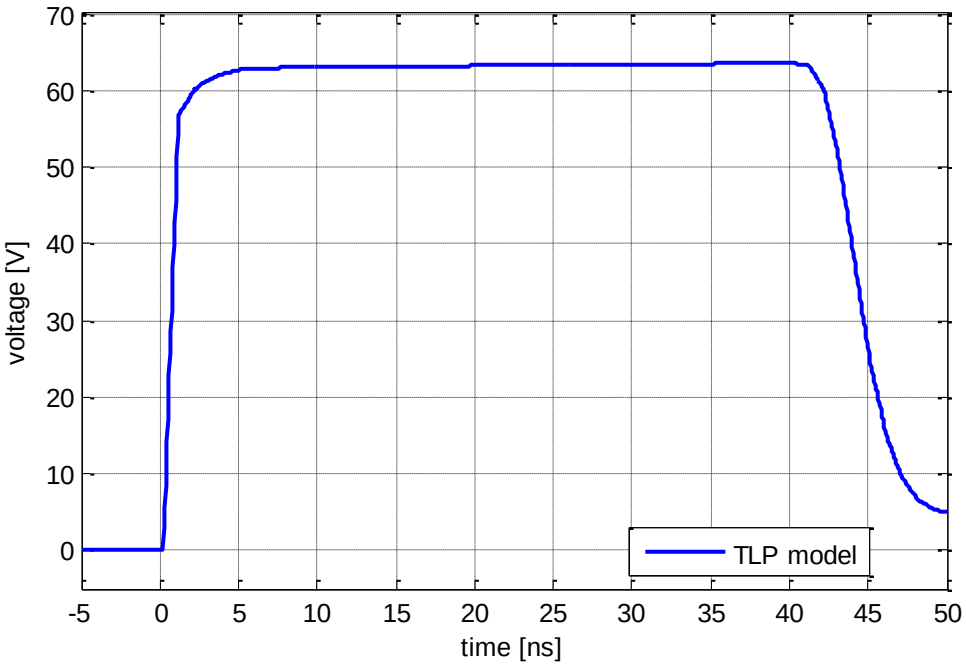

Figure 28: Simulated voltage of discharge of the TLP model into 50 Ω with 40 ns pulse width, 1,2 ns rise time and 1 kV charging voltage

2.2 PCB trace model (multi conductor transmission line model)

The transmission line models used for simulation of PCB structures are described in this section.

Multi conductor transmission line models can be applied for cross-talk simulation on PCBs. Detailed information on used models can be found in [10]. The simulation of

coupling effects is verified by a comparison to full wave simulation results. Figure 29 shows the equivalent circuit with two parallel conductors of equal length. A source is connected to one end of line 1. All wire endings are terminated with a 1 kΩ resistor. The source impedance is set to 50 Ω.

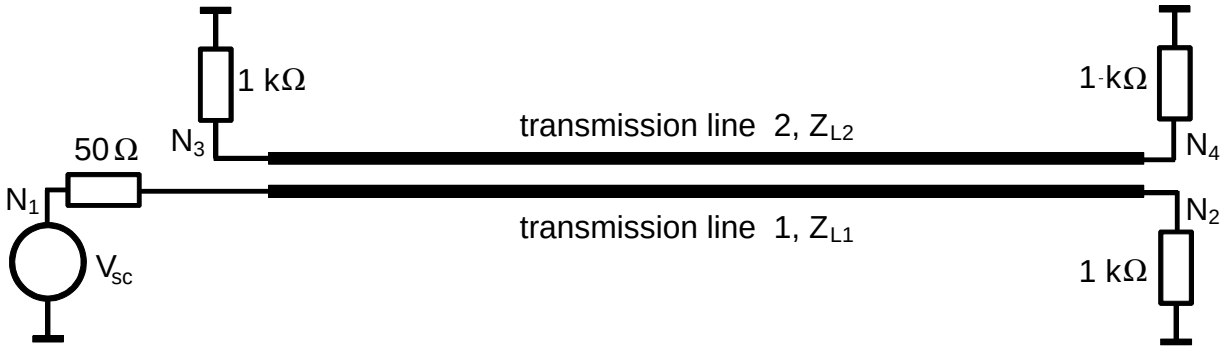

Figure 29: Setup for verification of transmission line models

In Figure 30 the 3D full-wave model is shown. Probes were set at nodes N_1, N_2, N_3 and N_4 as indicated in Figure 29. The distance between lines is 3 mm. The length of the conductors with radius 0,3 mm is 0,2 m and height above coupling plane is 3 mm.

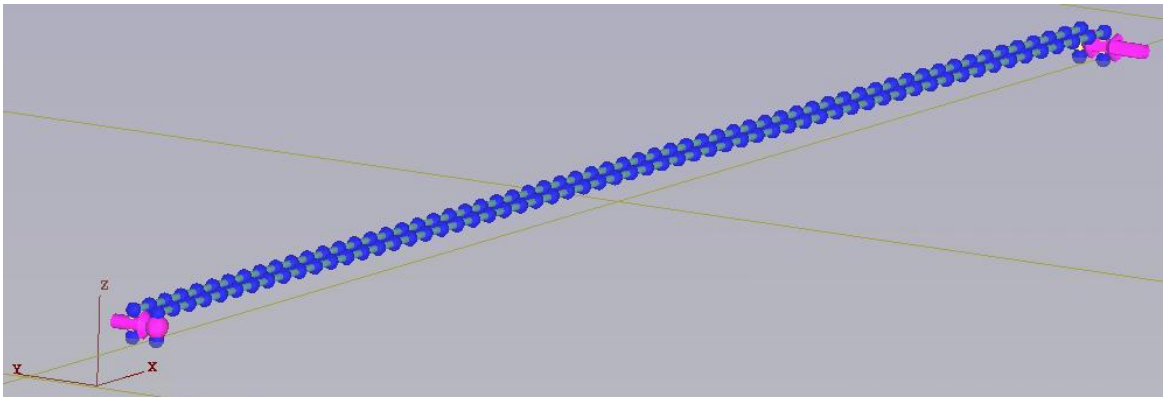

Figure 30: Full wave 3D simulation of transmission lines

The common mode and differential mode impedances of the transmission line configuration are extracted from the full wave model so that a similar setup can be implemented in VHDL-AMS concerning equal conductor lengths, transfer impedances and loads. Line parameters matrices are defined by the relation of the geometric configurations between transmission line 1, transmission line 2 and ground potential. The impedances can be calculated from L and C matrices. Detailed information can be found in [11].

$$L = \begin{bmatrix} 7.423\text{e-}07 & 2.819\text{e-}07 \\ 2.819\text{e-}07 & 7.422\text{e-}07 \end{bmatrix} \text{H}$$

$$C = \begin{bmatrix} 1.751\text{e-}11 & -6.653\text{e-}12 \\ -6.653\text{e-}12 & 1.752\text{e-}11 \end{bmatrix} \text{F}$$

The matrices are converted to modal parameters using transformation matrix T.

$$\mathrm{T} = \frac{1}{\sqrt{2}} \cdot \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$$

$$\mathrm{L}_{\mathrm{modal}} = \mathrm{T}^{-1} \times \mathrm{L} \times \mathrm{T}$$

$$\mathrm{C}_{\mathrm{modal}} = \mathrm{T}^{-1} \times \mathrm{C} \times \mathrm{T}$$

The modal values are used to calculate the modal impedance matrix Z_{modal}.

$$\mathrm{Z}_{\mathrm{modal}} = \sqrt{\frac{\mathrm{L}_{\mathrm{modal}}}{\mathrm{C}_{\mathrm{modal}}}}$$

The first element on the main diagonal of Z_{modal} represents Z_{even} and the second element Z_{odd}. Common mode and differential mode impedances are calculated using the following relations.

$$\mathrm{Z}_{\mathrm{com}} = \frac{1}{2} \cdot \mathrm{Z}_{\mathrm{even}}$$

$$\mathrm{Z}_{\mathrm{diff}} = 2 \cdot \mathrm{Z}_{\mathrm{odd}}$$

The values for Z_{com} and Z_{diff} for the given configuration were found and can be used as parameters in the VHDL-AMS model.

$$\mathrm{Z}_{\mathrm{com}} = 153{,}5\ \Omega$$

$$\mathrm{Z}_{\mathrm{diff}} = 276{,}0\ \Omega$$

The results of both simulations are compared in Figure 31 and Figure 32 in frequency domain. Very small deviations of around 1 % between the curves of full-wave and VHDL-AMS simulation results can be seen only at resonance frequencies.

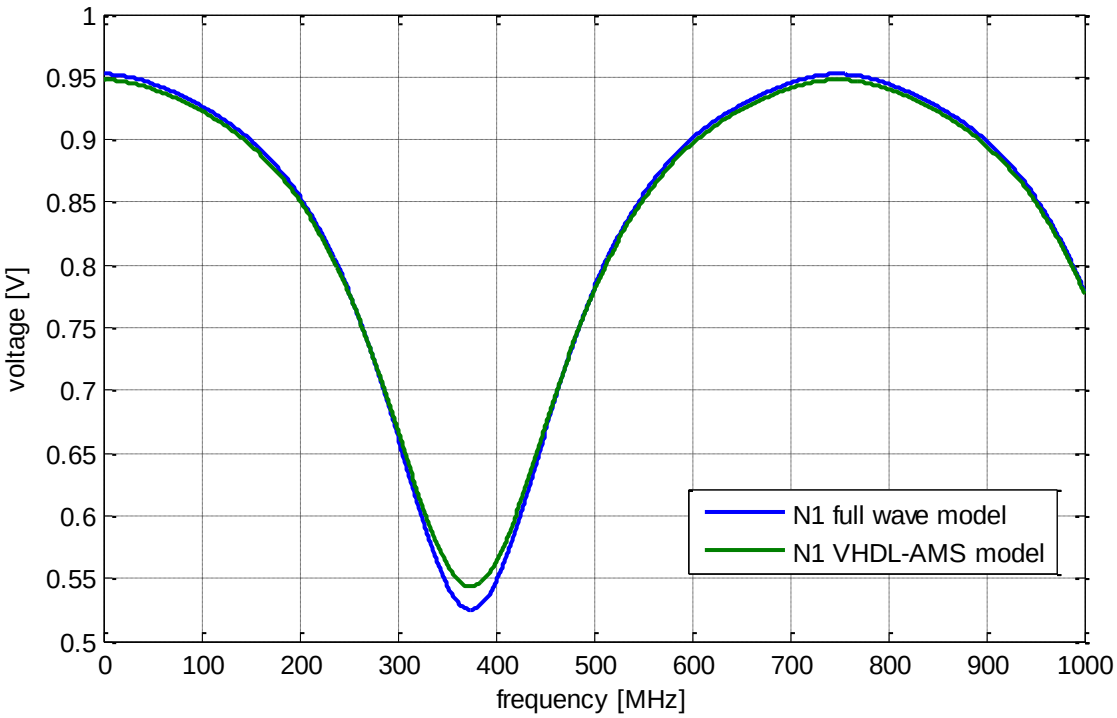

Figure 31: Comparison of VHDL-AMS and full wave simulation in frequency domain at node 1

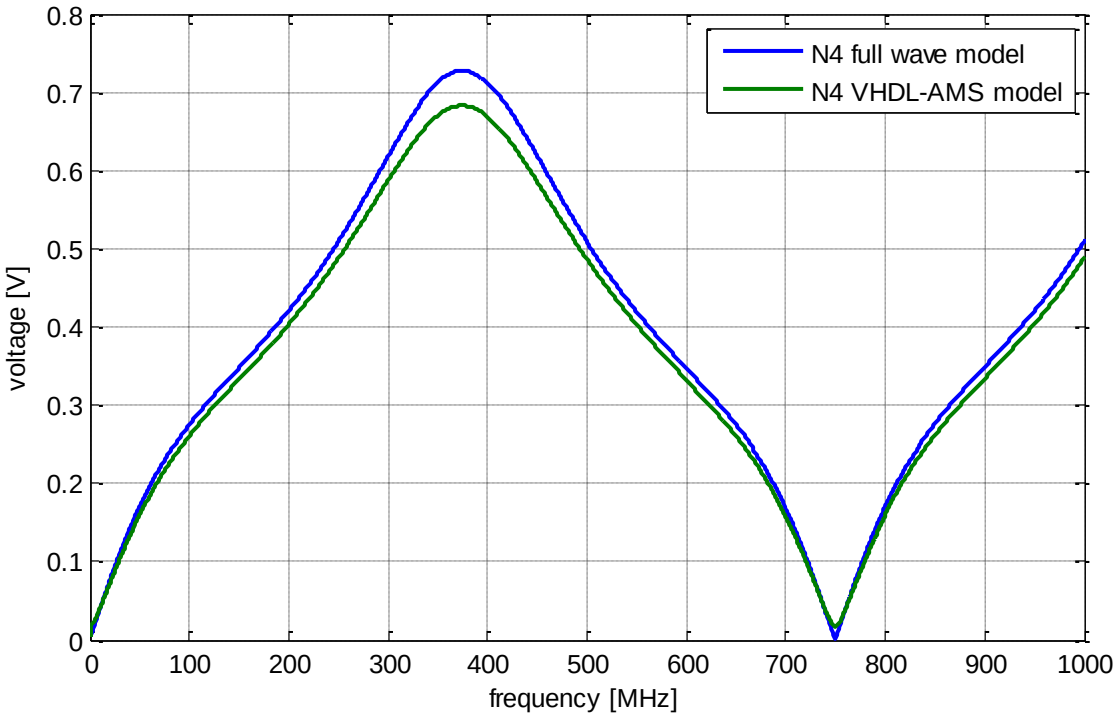

Figure 32: Comparison of VHDL-AMS and full wave simulation in frequency domain at node 4

In Figure 33 simulated waveforms are compared for a rectangular pulse with amplitude of 1000 V in time domain. Shown deviations are mainly caused by numerical problems of IFFT-algorithm of full wave solver.

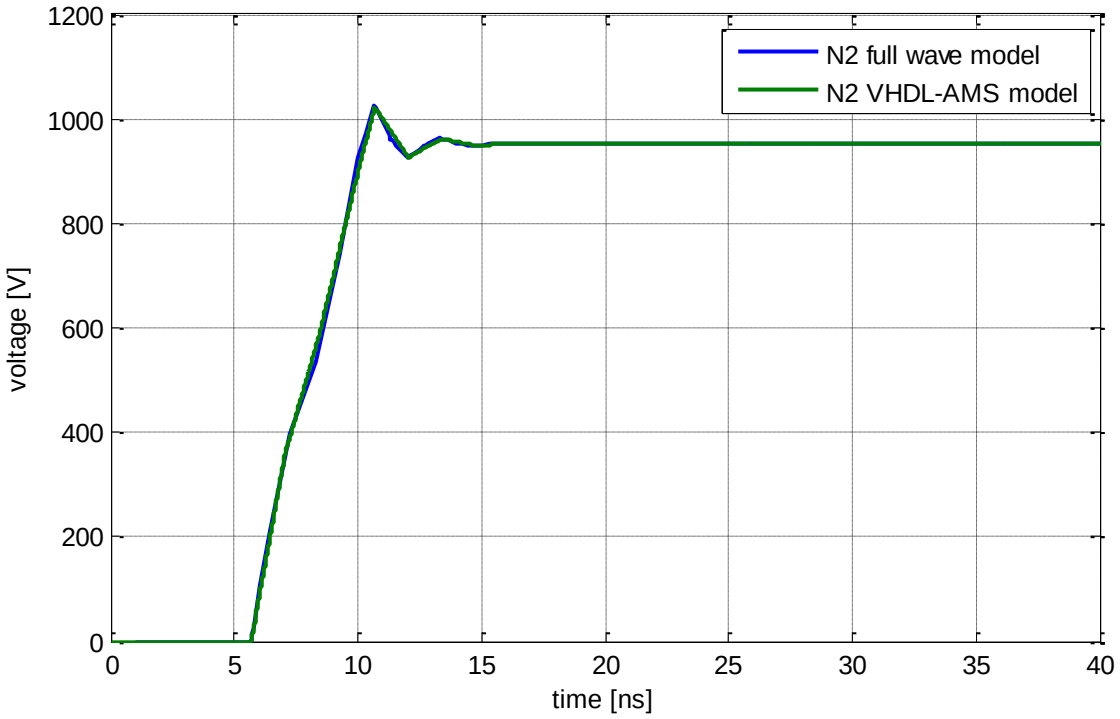

Figure 33: Comparison of full wave and VHDL-AMS model in time domain at node 2

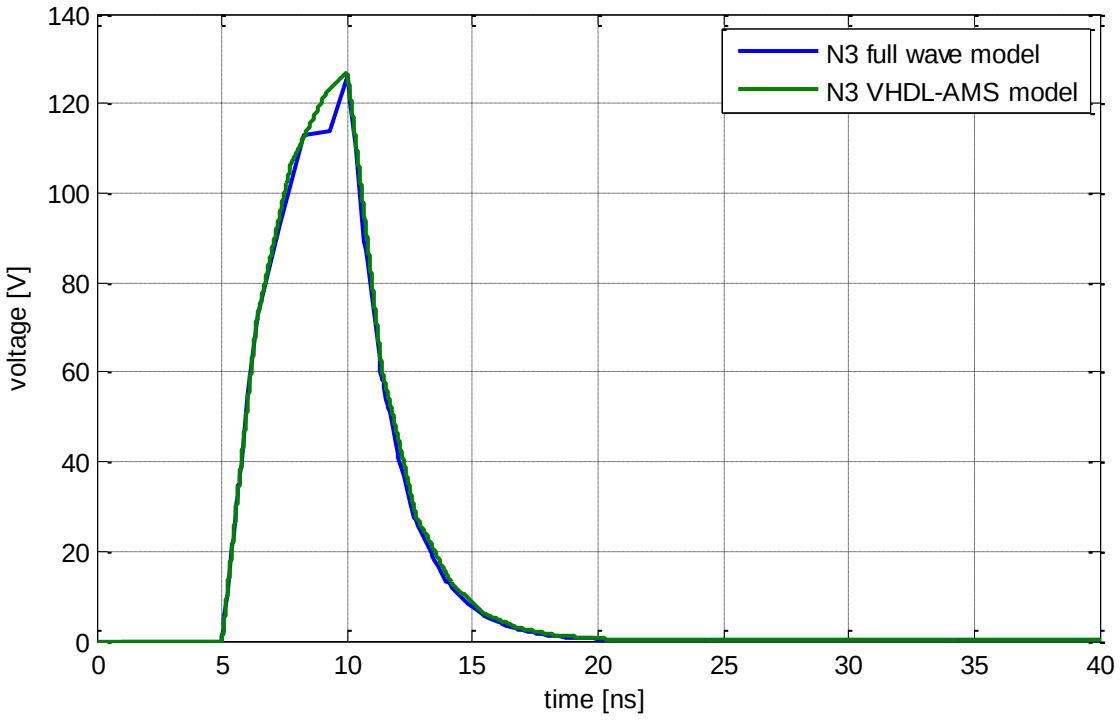

Figure 34: Comparison of full wave and VHDL-AMS model in time domain at node 3

2.3 Modeling of IC structures

A technique for ESD-failure modeling of IC structures is described in this section. More information can be found in [12]. In section 2.3.1 a general approach for

modeling the static and dynamic electrical behavior of unpowered ICs-pins is explained. The general technique is limited to the electrical domain. A second approach focuses on the modeling of the thermal ESD robustness of ICs is described in section 2.3.2.

The modeling approach is based on a pragmatic behavioral modeling technique without any information about IC parameters such as geometry of package, die structure, and so on.

2.3.1 **General modeling approach for electrical domain**

For modeling characterization data have to be measured. The IV-characteristic of a device is measured for low currents with an IV-source meter [13] and for high currents up to 60 A with a TLP [7]. In Figure 35 an equivalent circuit of the measurement setup is shown. Attenuation factors for voltage and current can be calibrated using the HPPI software. The TLP current and voltage waveforms are measured with an oscilloscope. A Tektronix CT1 current sensor is connected to measure I_{meas}. An additional resistor R_s is soldered in the branch to the oscilloscope for attenuation. The voltage V_{meas} can be calculated with knowledge of all attenuation factors from V_{osc}.

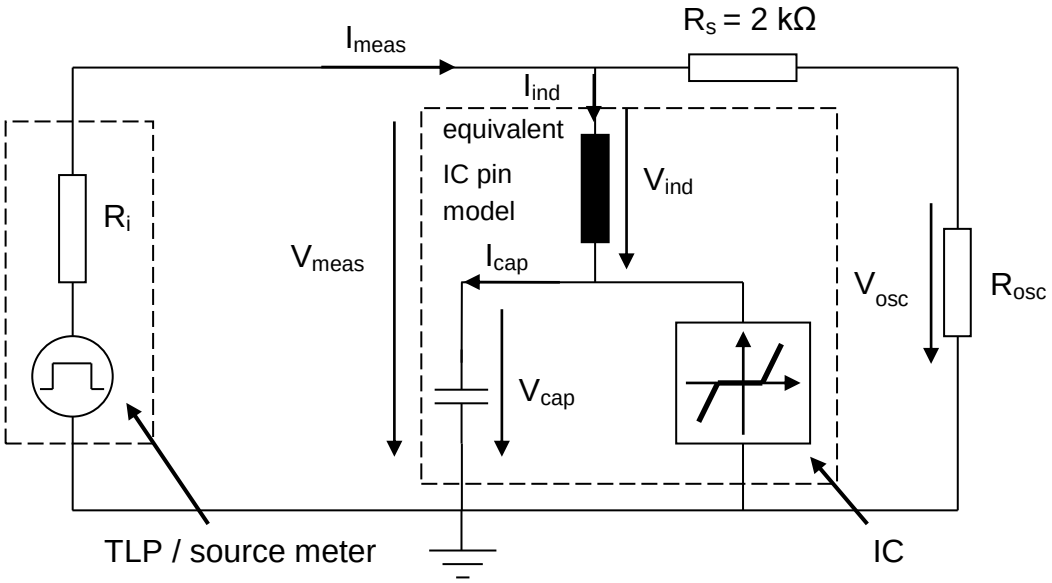

Figure 35: Measurement setup for characterization of ICs and behavioral model for an IC pin

The equivalent circuit of each IC pin is composed of elements which describe the static behavior and of those which describe the dynamic behavior.

The general equivalent circuit describing the electrical domain of the IC is shown in Figure 36. The frequency dependent parameters are measured with a network analyzer to define the size of the capacitance $C_{parallel}$ and inductance L_{serial} of an IC pin. The characteristic IV curve is composed from the source meter and TLP measurement data. The IV behavior is implemented in the model using a look-up

table function. To generate reliable measurement data minimum two equal ICs have to be tested until destruction. Deviations between the failure levels must be low. Good results were obtained with a pulse width of 100 ns. The measurement data can be extrapolated if higher amplitudes should be simulated. Due to missing verification of this model region a warning will be returned by the model.

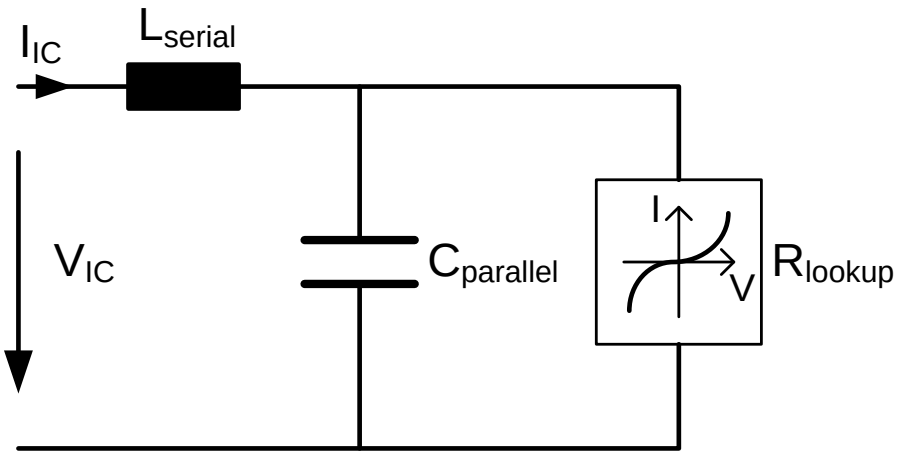

Figure 36: IC pin model für ESD failure analysis

The IC pin model can also be used for modeling of ESD-protection devices. Figure 37, Figure 38 and Figure 39 show an example of a composed IV-dataset of a varistor. Data in a dynamic range from nA up to 50 A are obtained by measurement.

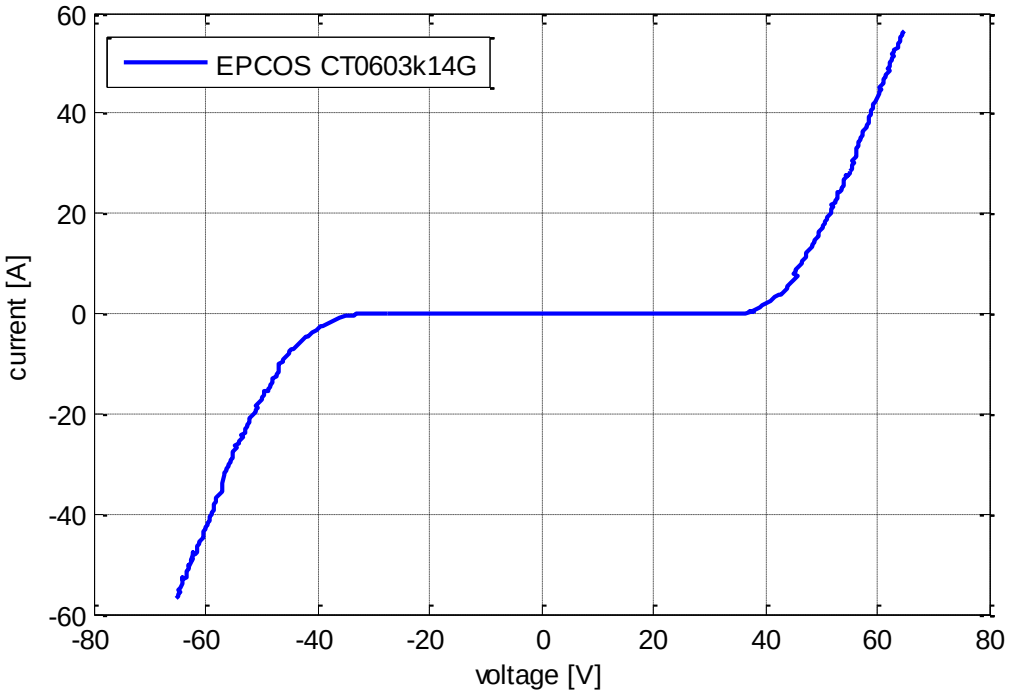

Figure 37: Composed varistor IV-curve

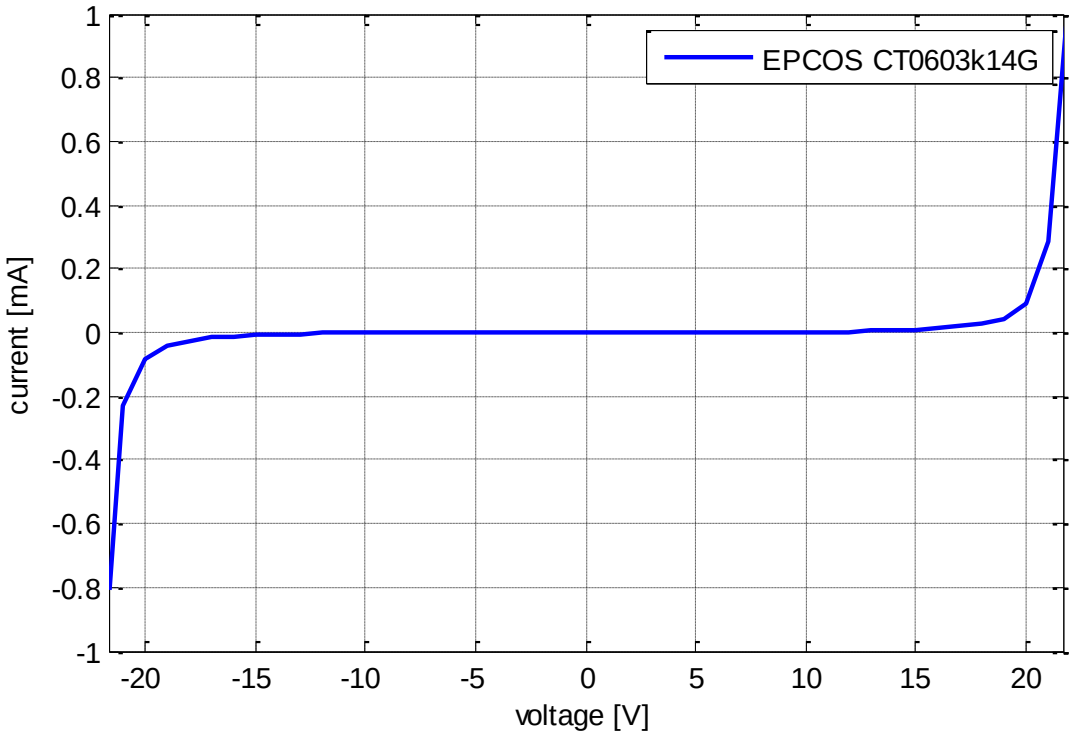

Figure 38: Composed varistor IV-curve in detail

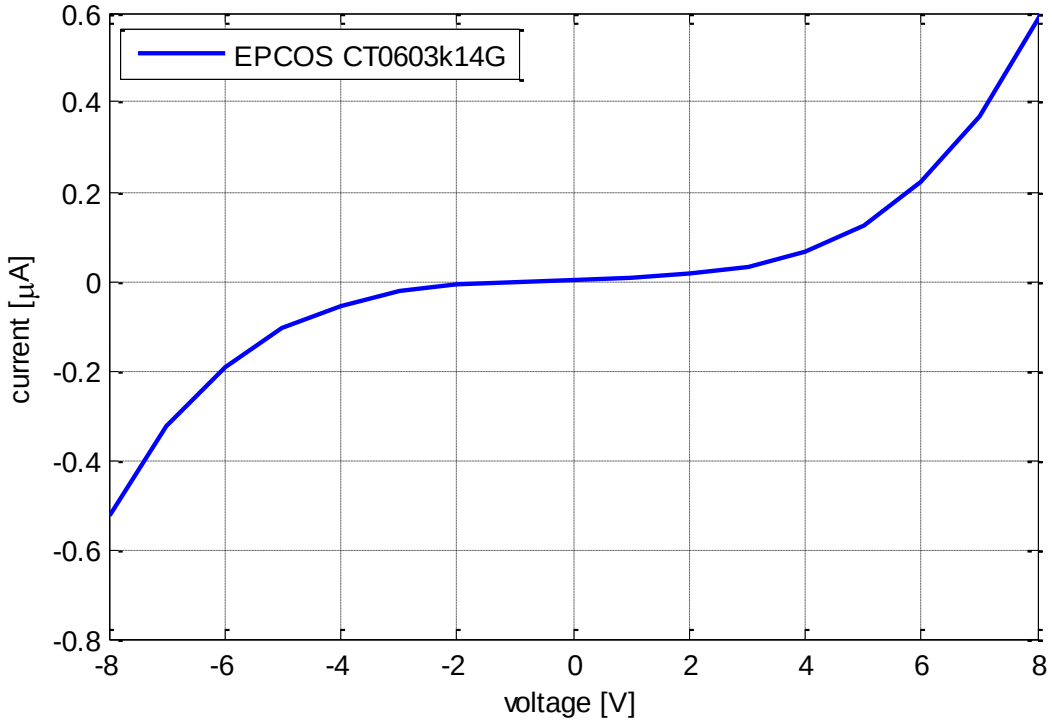

Figure 39: Exact modeling of varistor for low voltage behavior

Some protection circuits show a snap-back effect. ICs can be protected using snap-back of the IV curve. If a voltage level is exceeded a breakdown of the voltage occurs. Current amplitudes are rising. The IV curve in Figure 40 shows a snap-back around 250 V for positive and negative amplitudes.

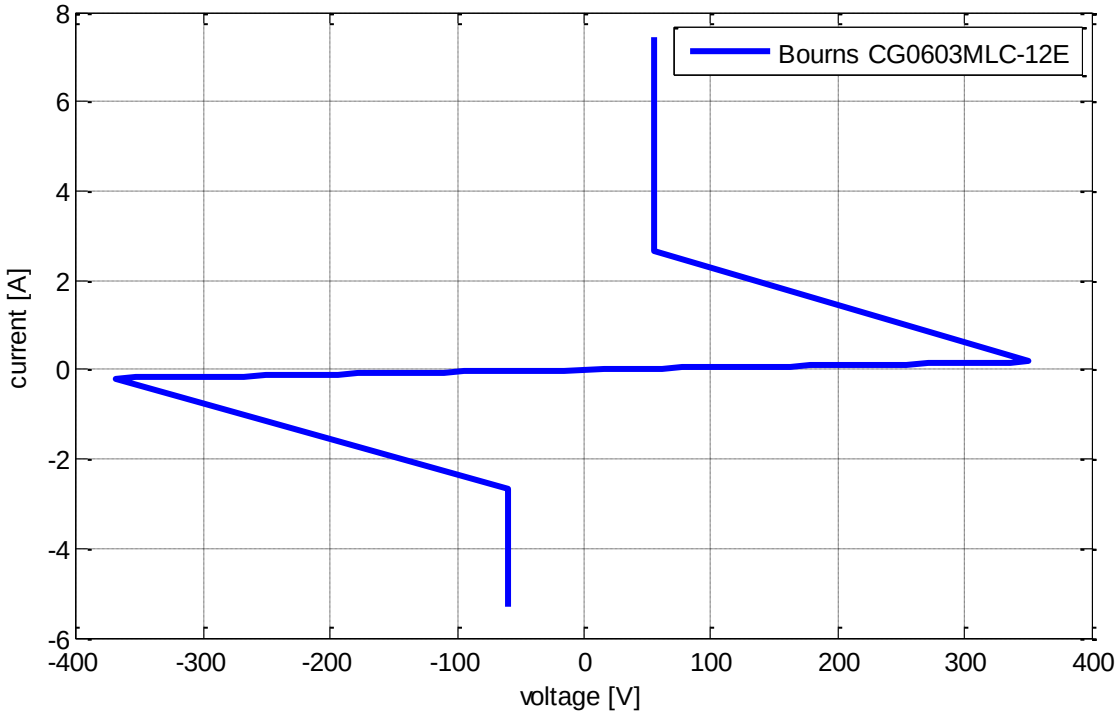

Figure 40: Measured IV characteristic of a polymer protection device

Snap-back effects cannot be implemented with a single lookup-table because of continuity problems. For modeling a second dataset has to be composed containing measurement data after the breakdown. In Figure 41 the switch S_1 is closed if the defined value of breakdown voltage is exceeded. A more complex implementation is possible if hysteresis functions are considered.

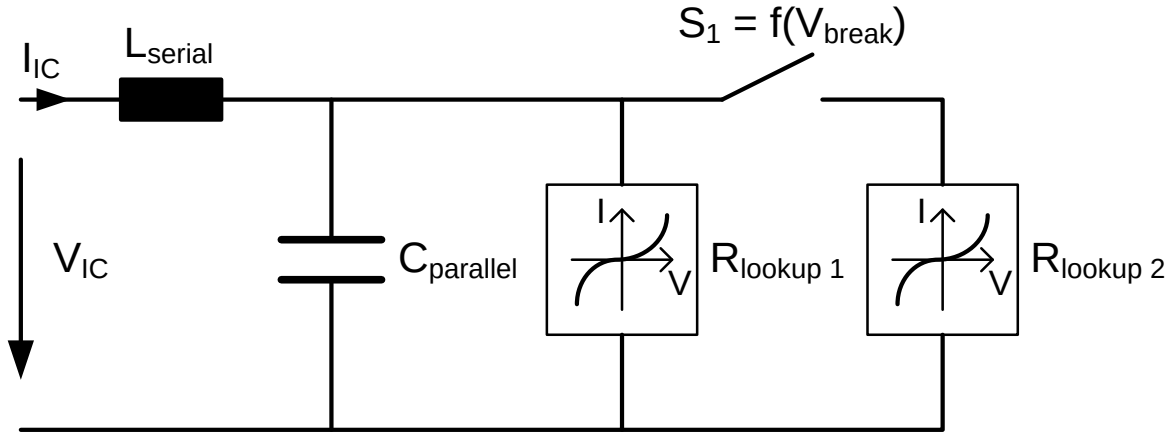

Figure 41: ESD protection element model with snap-back

2.3.2 **Thermal failure model**

IC failure can often be referred either to a critical voltage or a critical temperature. In case of critical voltage a dielectric breakdown due to high local field strength inside the semiconductor occur. Here failure voltage is the critical parameter and should be

constant. Thermal failures are energy dependent. In the adiabatic region failure energy should be constant.

ESD currents flowing through the semiconductor have to be considered. The absolute active surface affected by ESD pulses usually is unknown and can only be estimated if it is assumed that total current passes through local hot spots in the semiconductor leading to destruction of the IC. Different approaches were developed to describe a power or energy dependent process leading to permanent damage condition. Wunsch-Bell described the heating of a structure as a heat source inside an infinite volume [14] [15]. Furthermore the heat flow process is assumed to be one dimensional. For rectangular pulses with duration times around 100 ns up to microseconds heat transfer from the current constriction site in the IC is assumed to be minimal.

Wunsch-Bell is based on a 2-dimensional thermal model based on power area. If all material constants are temperature-independent the specific power P_f is calculated from the following equation to reach a critical temperature T_c.

$$P_f = \sqrt{\pi \kappa \rho c_p}\,(T_c - T_0) \cdot t_p^{-\frac{1}{2}}$$

κ	Thermal conductivity:	30,6 W/mK (for Si)
c_p	Specific heat capacitance:	756,6 J/kgK (for Si)
ρ	Specific density:	2330 kg/m^3 (for Si)
T_0	Environment temperature:	293 K
T_c	Critical temperature:	1685 K
t_p	Pulse width:	from 100 ns up to 20 µs

Under these conditions the failure power per area decreases with increasing pulse width t_p. Often the critical temperature is estimated. For the investigations the melting temperature of silicon was chosen.

2.3.2.1 Adiabatic RC model

IC failure models are implemented in VHDL-AMS in thermal domain. The power at the IC pin is transformed into a heat source in thermal domain. In Figure 42 the source indicated with P_{th} is connected to a thermal capacitor C_{th} and resistor R_{th}.

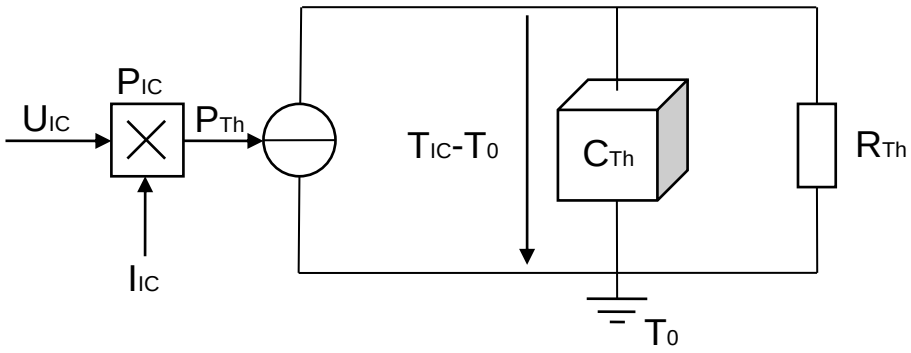

Figure 42: Thermal domain of IC model

The simulated temperature rise $T_\Delta = T_{IC}-T_0$ is obtained as a function of all thermal components in the circuit and from the environment temperature $T_{0.}$

$$P_{Th} = C_{Th} \cdot \frac{dT_\Delta(t)}{dt} + \frac{T_\Delta(t)}{R_{Th}}$$

A defined critical temperature T_c is reached for a certain failure power P_{TLP} obtained from TLP measurement with the pulse width t_{TLP}. All models are based on TLP data with a selected pulse width of 100 ns because measured critical energies will change with variable pulses width. The thermal capacitance is calculated using the following equation.

$$\boldsymbol{C_{Th} = -\frac{t_{TLP}}{R_{Th} \cdot ln\left(1 - \frac{T_C - T_0}{P_{TLP} \cdot R_{Th}}\right)}}$$

Dissipation is controlled by the thermal resistance R_{th} which is difficult to estimate because failed chips could not be analyzed and the active area after Wunsch-Bell may change due to local hot spots inside the semiconductor. The active area may decrease to 1/10. This means that the thermal resistance also is affected. For modeling R_{th} should be chosen in accordance with the type of the IC. Dimensions of silicon structures inside ICs with higher ESD robustness are supposed to be larger than inside “ESD-weak” ICs. Thermal resistance R_{th} therefore should be lower for extended structures and higher for smaller active areas.

For simplification the structures in semiconductors are supposed to be in general very simple and identical like shown in Figure 43.

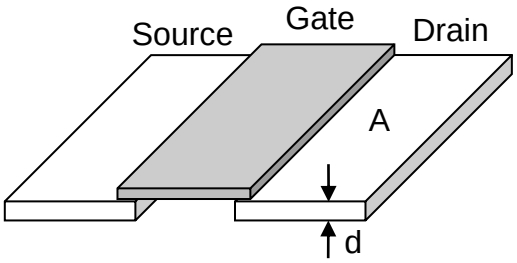

Figure 43: Planar structures in semiconductors

The thermal capacitance C_{th} and resistance R_{th} then are both dominated by the surface A. This gives another possibility to compute the thermal capacitance from material constants:

$$C_{Th} = \rho \cdot c_P \cdot A \cdot d$$

Also the thermal resistance can be calculated:

$$R_{Th} = \frac{d}{k \cdot A}$$

κ	thermal conductivity
c_p	specific heat capacity
ρ	specific density

2.3.3 **Scaling of the IC ESD robustness**

Once the µC, LIN and CAN models parameters of the test chips are known and the models are verified, the thermal behavior of the models can be modified and the failure levels can be changed in order to simulate different robustness levels.

When scaling down the current-carrying capacity of semiconductor models the thermal capacity decreases. This is equivalent to a downscaling of the dimensions of the IC's ESD protection circuit which also has impact on the thermal resistance R_{th}.

To avoid unbalanced heat dissipation of failure models with scaled thermal domain, the time constant τ of R_{th} and C_{th} is assumed to be constant:

$$\tau = R_{th} C_{th} = const$$

This means that the scaling factors are calculated related to a certain pulse energy where the scaled model is supposed to show a given failure behavior. Scaling for a new testing device or a new failure level is performed according to the following steps:

1. Simulate the absorbed energy at the IC pin for a new testing device or charging voltage level
2. Calculate the factor between the energy obtained for the new testing level and the original IC model
3. Divide the original thermal capacitance and resistance by the factor from (2)

3 Characterization of selected devices

The characterization results of selected devices for the investigations are presented in this section. Measurement and simulation data of ESD protection elements and IC pins are compared in section 3.1 and 3.2. The calculated parameters of the models with reduced ESD robustness are presented in section 3.3.

3.1 Selected ESD protection devices

ESD-protection devices can be soldered in parallel to the IC pins to increase the ESD robustness of a circuit. A general technique and the modeling of ESD-protection elements is described in [14].

For investigations described here 10 models (capacitor, varistors, TVS diodes) of ESD protection elements were developed. Important characteristic data of all devices is listed in Table 4.

Type	**Identifier**	**V_{clamp} (600 V TLP)**	**$C_{parallel}$**	**L_{serial}**
Capacitor	EPCOS 10 nF 0805 X7R	-	10 nF	1 nH
Varistor	Vishay MLV0603E30403T	32 V	700 pF	3,2 nH
	TDK AVR-M1608C180M	33 V	480 pF	2,7 nH
	EPCOS CT0603K14G	50 V	120 pF	7,5 nH
	AVX VC060318A400	61 V	120 pF	8,1 nH
	EPCOS CT0603S14AHSG	81 V	20 pF	6,7 nH
Diode	Protek TVS GBLCS05C-LF	16 V	3 pF	5,4 nH
	NEC NNCD12D-A	17 V	35 pF	2,6 nH
	Taiwan Semiconductor TSZU52C18	25 V	20 pF	2,3 nH
	Bourns CD0603-T12C	35 V	9 pF	3,4 nH

Table 4: External ESD protection elements

3.1.1.1 Varistors

The measured voltage and current waveforms of the selected varistors are shown in Figure 44 and Figure 45. Differences in the clamping and peak voltage of more than 100 % between the curves are obtained. Deviations between current amplitudes are less than 10 %.

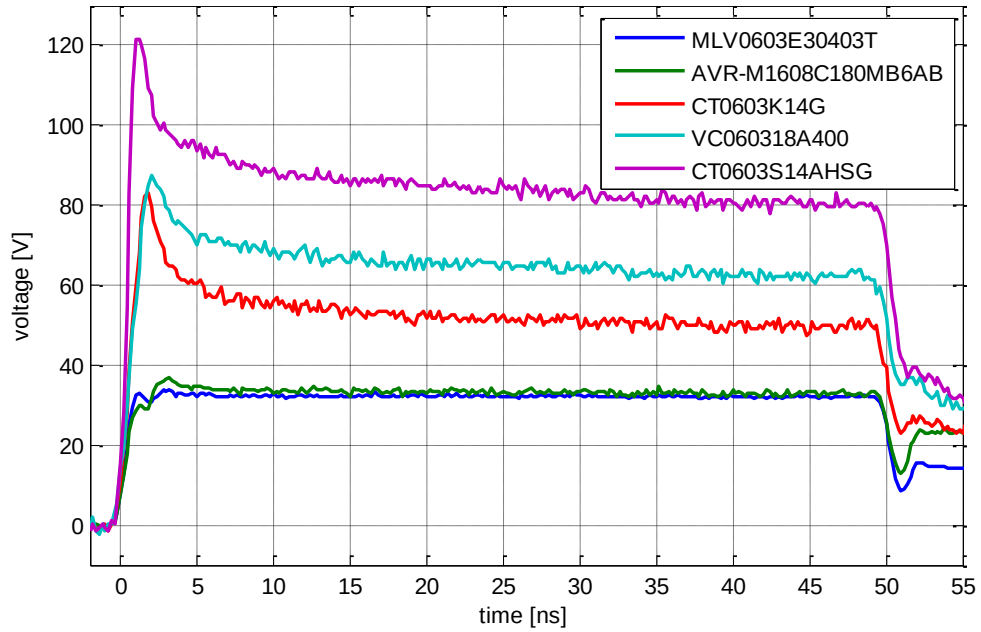

Figure 44: Comparison of measured voltage waveforms of different varistors for 600 V TLP charging voltage

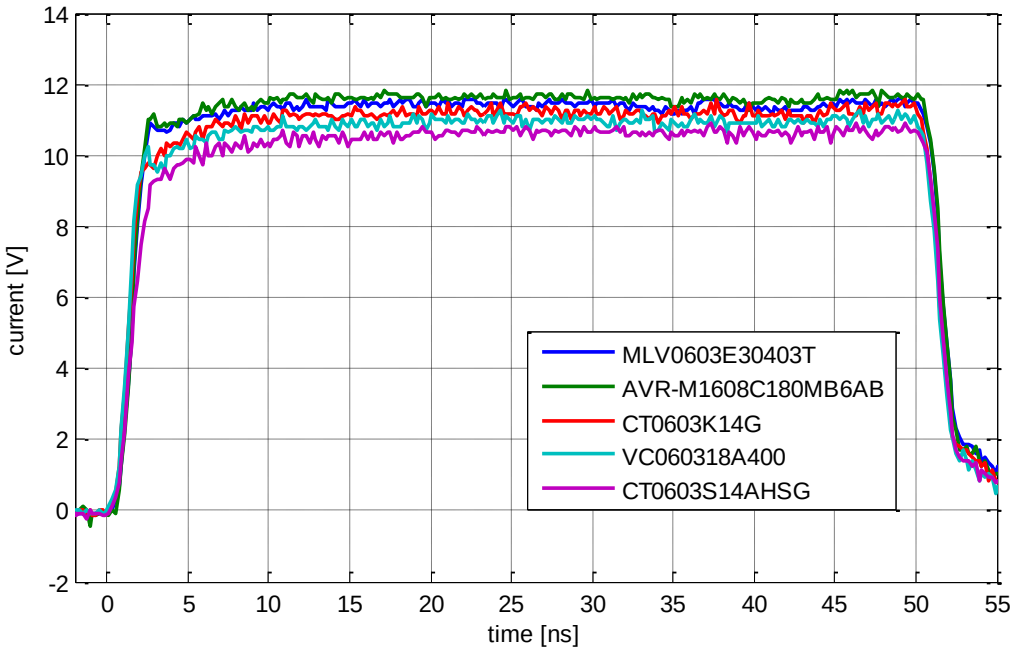

Figure 45: Comparison of measured current waveforms of different varistors for 600 V TLP charging voltage

The breakdown voltages of the devices can be extracted from the IV-curves in Figure 46 and Figure 47. Although the clamping voltages of some devices are similar the breakdown voltages can be different.

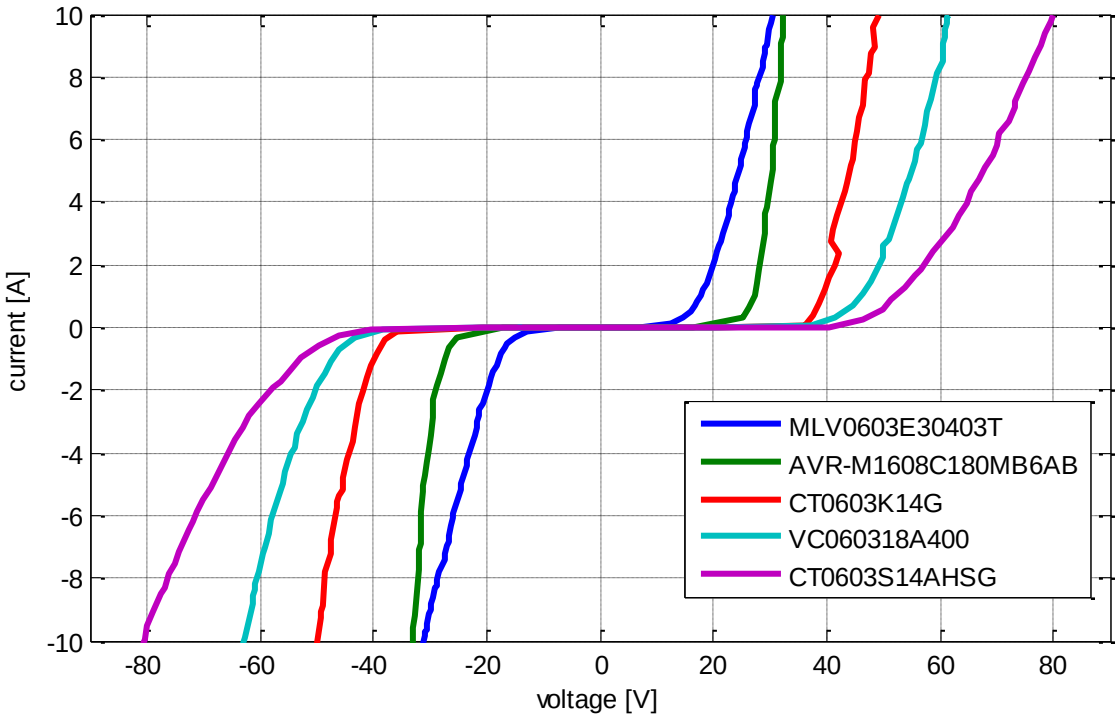

Figure 46: Comparison of IV-curves of varistors measured with TLP

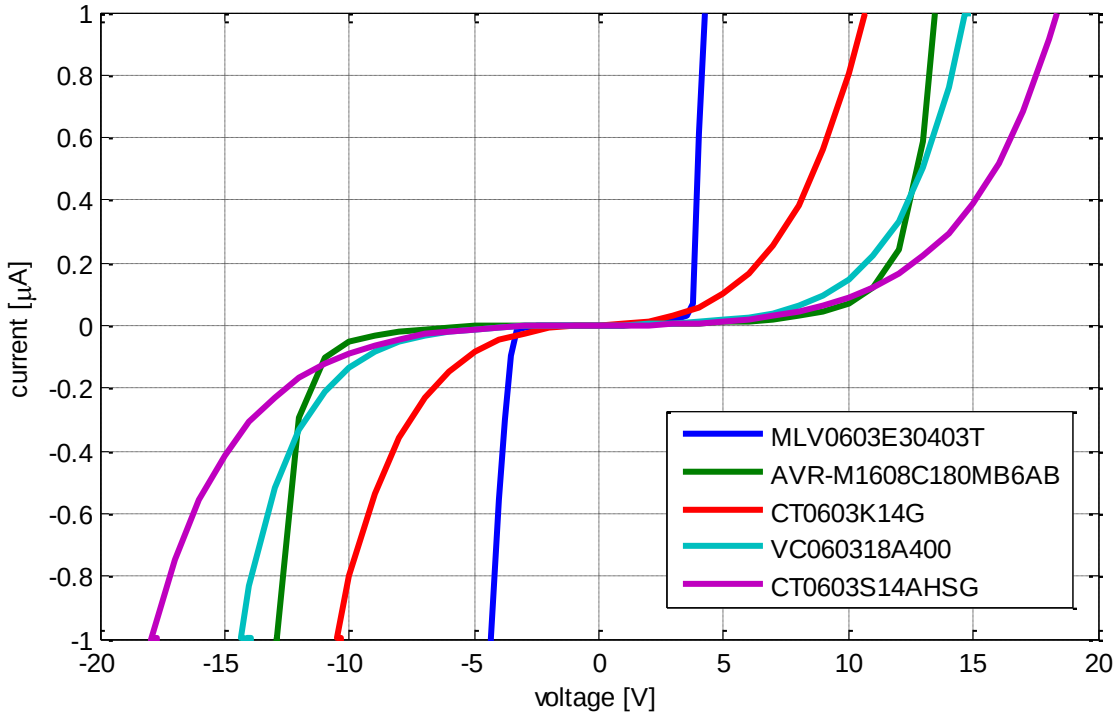

Figure 47: Comparison of IV-curves of varistors measured with TLP (low voltage region in detail)

The quality of a model can be verified by simulating the TLP measurement setup. Figure 48 and Figure 49 show the voltage and current waveforms for a 600 V TLP discharge and a TDK varistor exemplarily. All rise times, fall times, and clamping behavior are modeled with less than 5 % deviation.

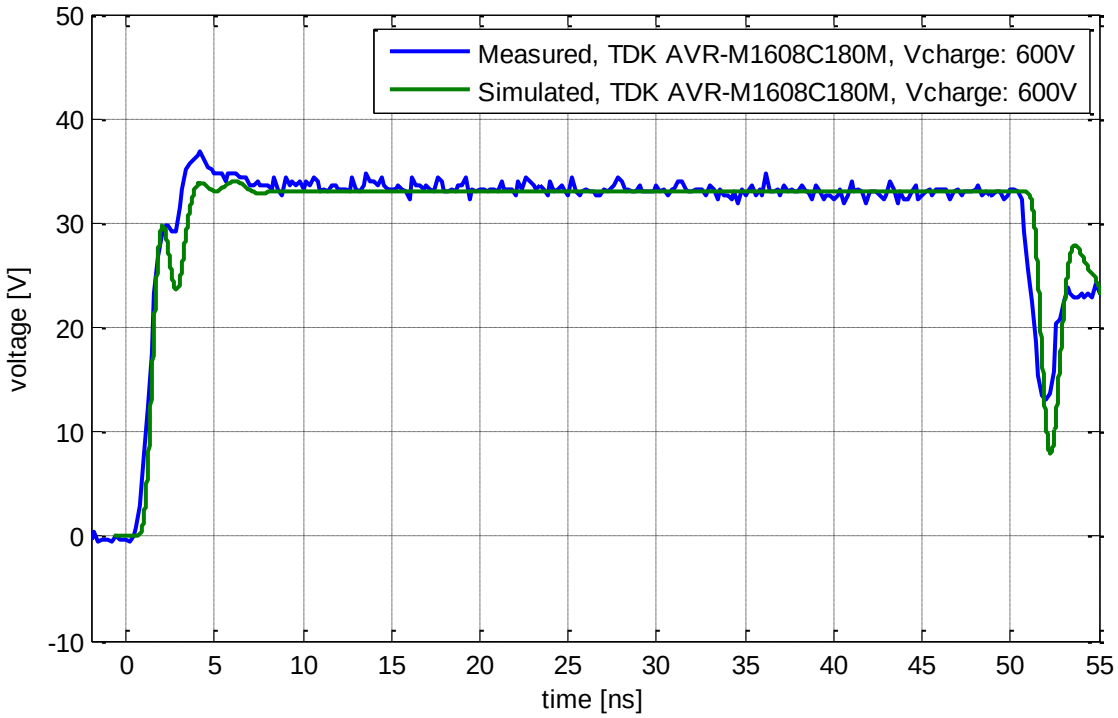

Figure 48: Comparison of measured and simulated TLP voltage with TDK varistor

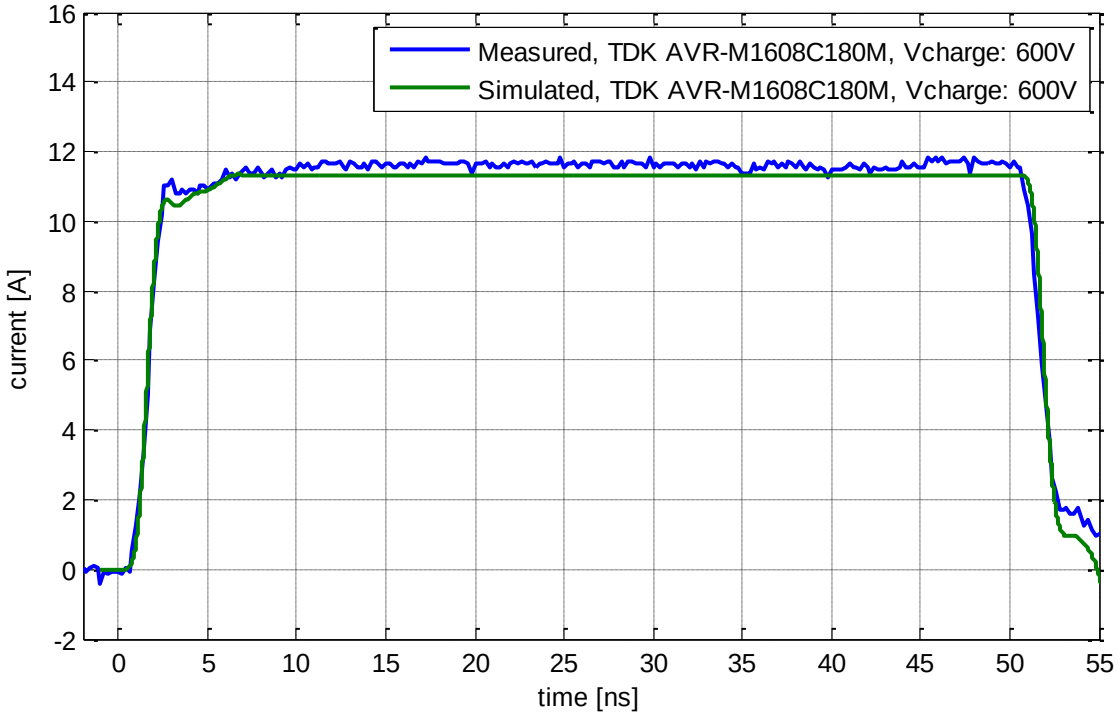

Figure 49: Comparison of measured and simulated TLP current with TDK varistor

3.1.1.2 Diodes

Voltage and current waveforms of the selected TVS diodes are compared in Figure 50 and Figure 51. In comparison to varistors the clamping voltage is lower. Lower

capacitances than 35 pF were measured for all diodes. The measured IV-plots show that 3 of the 4 investigated diodes are non-symmetric.

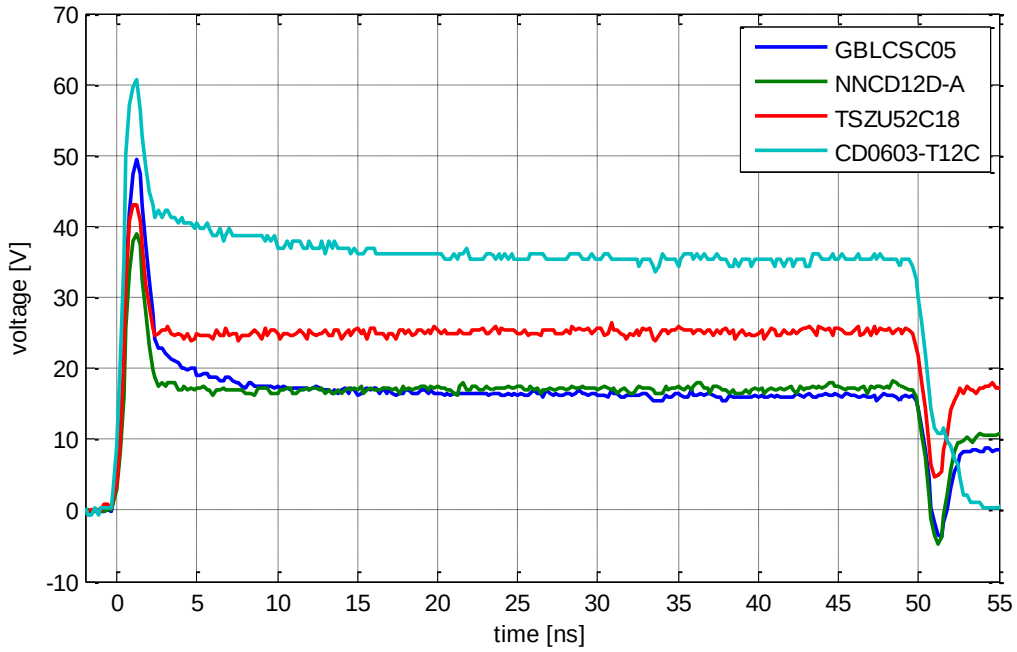

Figure 50: Comparison of measured voltage waveforms of different TVS diodes

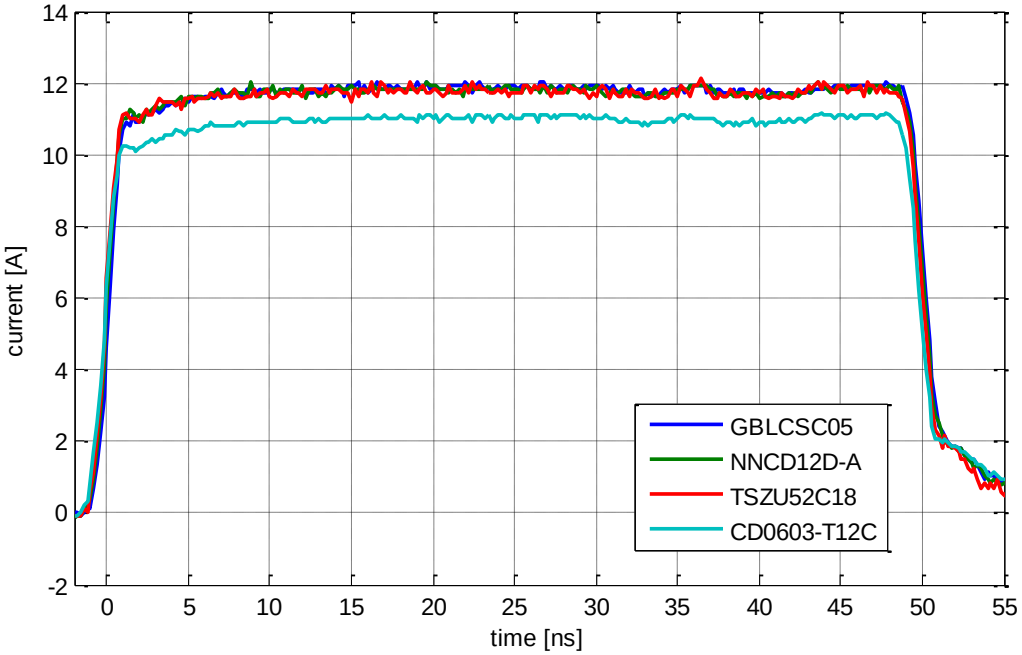

Figure 51: Comparison of measured current waveforms of different TVS diodes

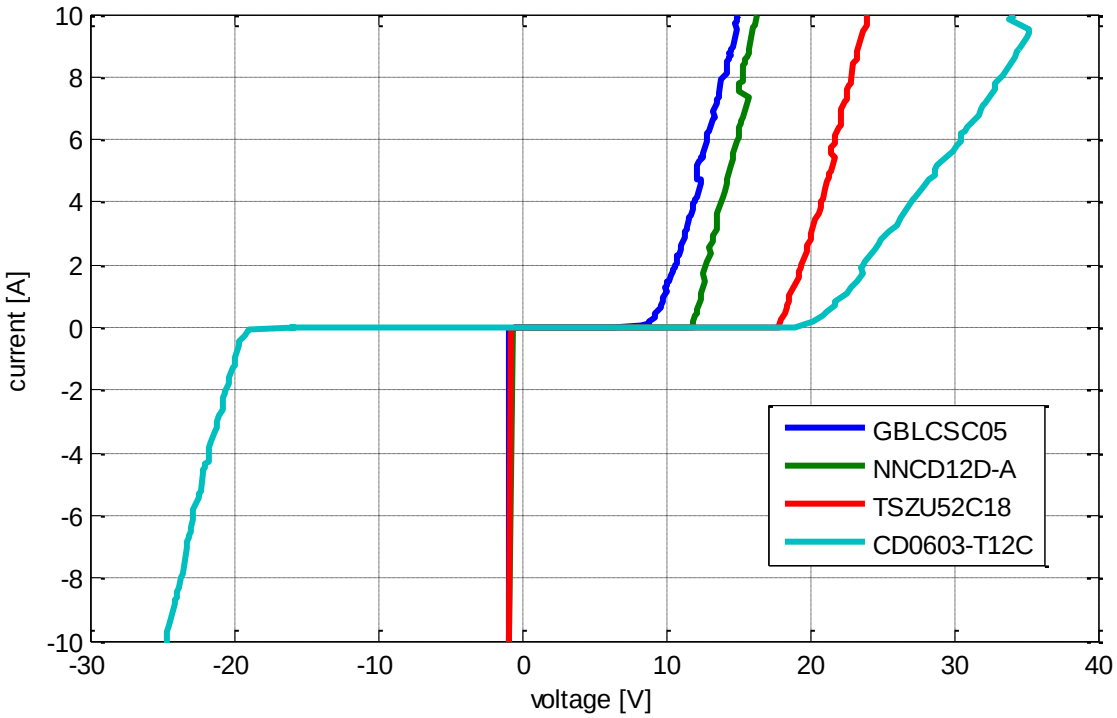

Figure 52: Comparison of IV-curves of diodes measured with TLP

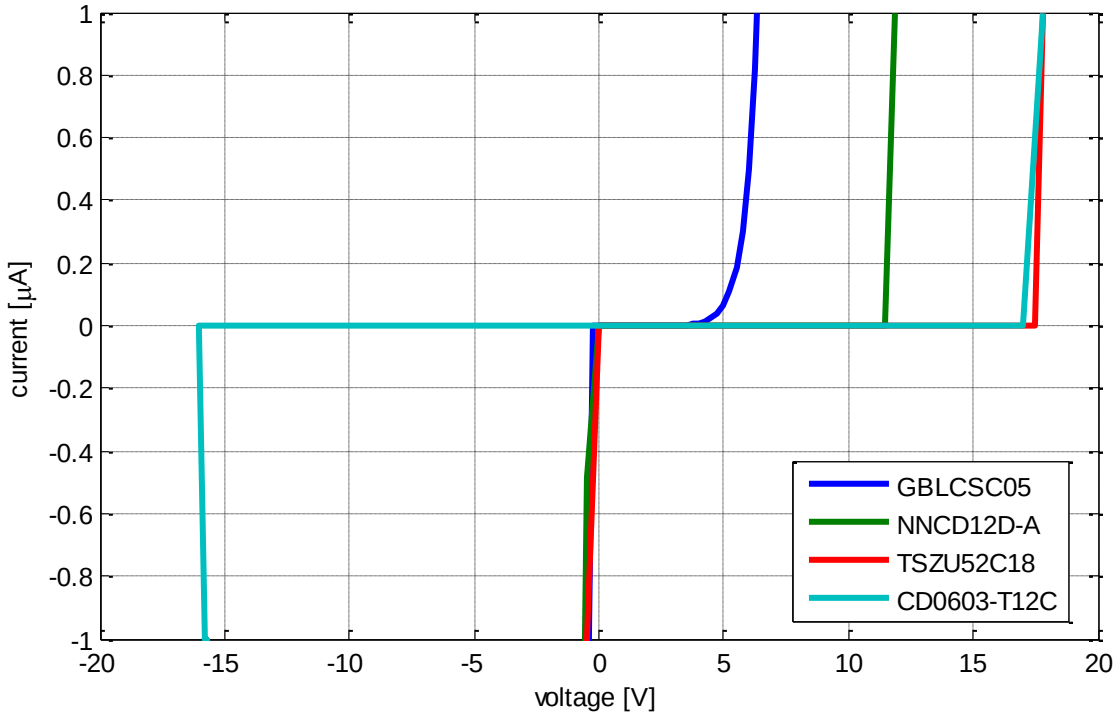

Figure 53: Comparison of IV-curves of diodes measured with TLP in detail

In Figure 54 and Figure 55 the measured and simulated waveforms with an NEC diode connected to the TLP setup are plotted. Good accuracy with less than 5 % deviation is obtained for TVS diode models.

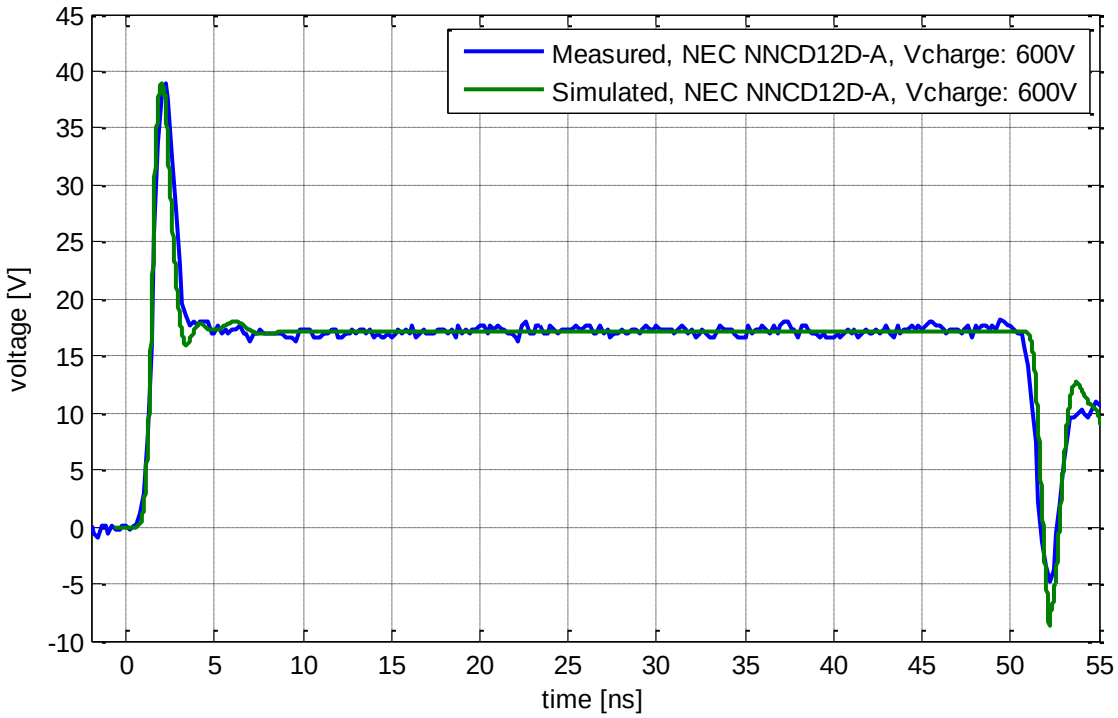

Figure 54: Comparison of measured and simulated voltage at NEC TVS diode

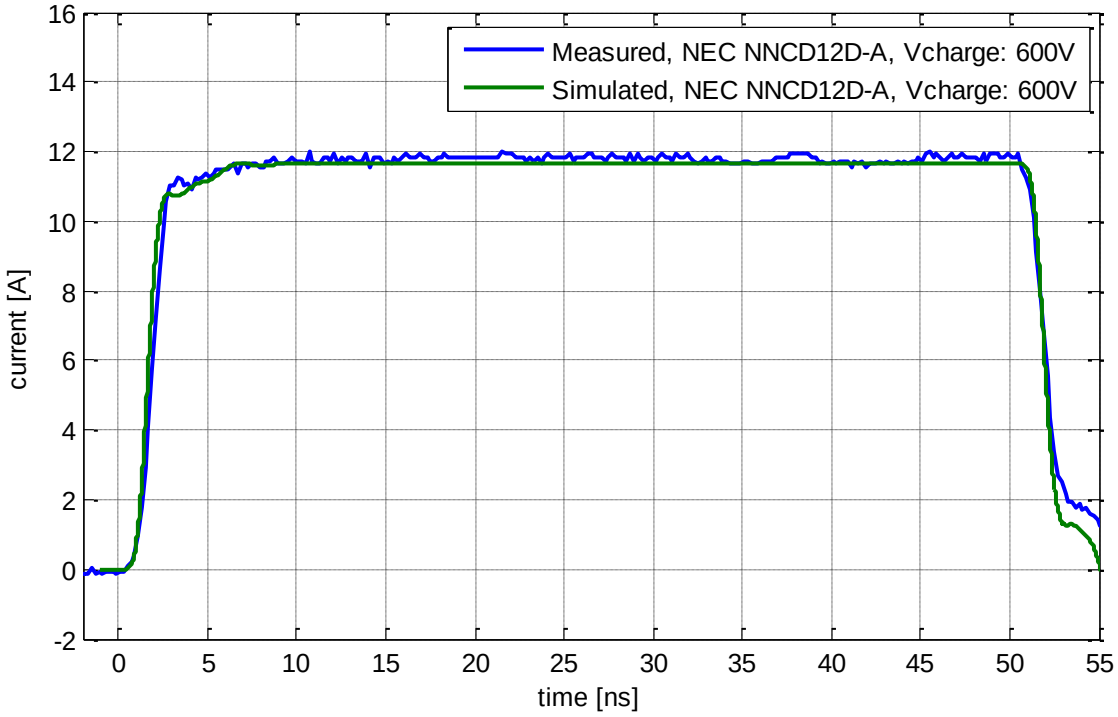

Figure 55: Comparison of measured and simulated current at NEC TVS diode

3.2 Characterization of selected IC pins with TLP

The characterization data for the selected IC pins is measured with two measurement setups. The TLP measurement setup shown in section 3.2.1 was used in time domain. A frequency domain setup with a network analyzer is described in

section 3.2.2. In the following sections 3.2.3, 3.2.4 and 3.2.5 waveforms and IV curves are presented for a LIN ATA6662C transceiver, CAN TJA1041T transceiver and a XC864 microcontroller. For verification of the measurement data and the created model simulated and measured waveforms are compared.

3.2.1 Time domain measurement setup

The time domain characterization setup shown in Figure 56 is controlled via a PC which is connected to the TLP unit, a fast 6 GHz 20 GS/s oscilloscope, and a source meter with minimal current resolution of 10 pA. All instruments are connected to the test board by a switch.

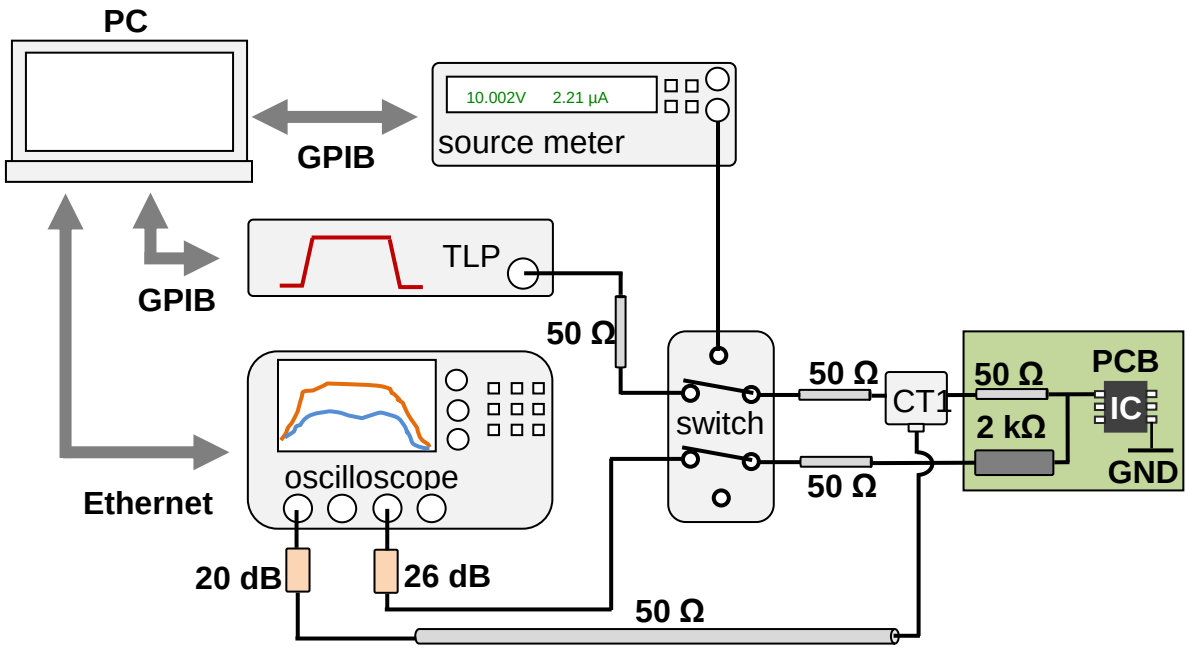

Figure 56: Measurement setup for IC characterization

For the investigations two test boards were developed. On the board shown in Figure 57 selected socket pins for CAN and LIN transceivers are connected via short traces to SMA connectors for measurement. Each selected pin for characterization is independent so that all SMA connectors are left open on the board except two used for measurement. Current is measured with a CT1 current sensor. Voltage and current amplitudes are attenuated by minimum 20 dB in order to protect measurement devices.

Figure 58 shows the equivalent test board with a socket for the µC. During measurement the PCBs were screwed on a metal plane to ensure adequate grounding conditions.

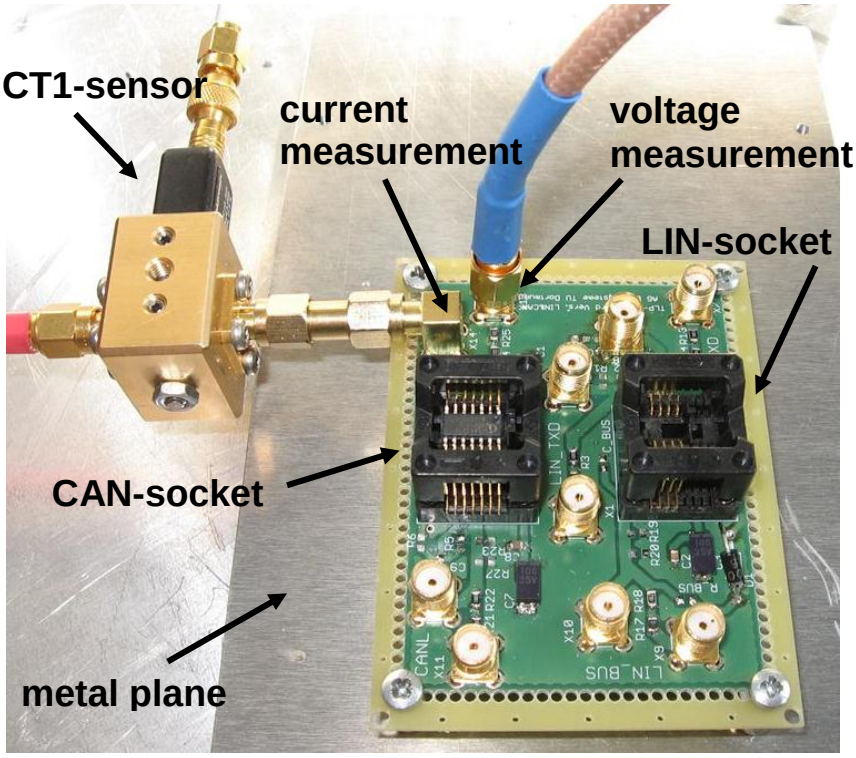

Figure 57: TLP measurement setup with PCB for LIN and CAN transceivers

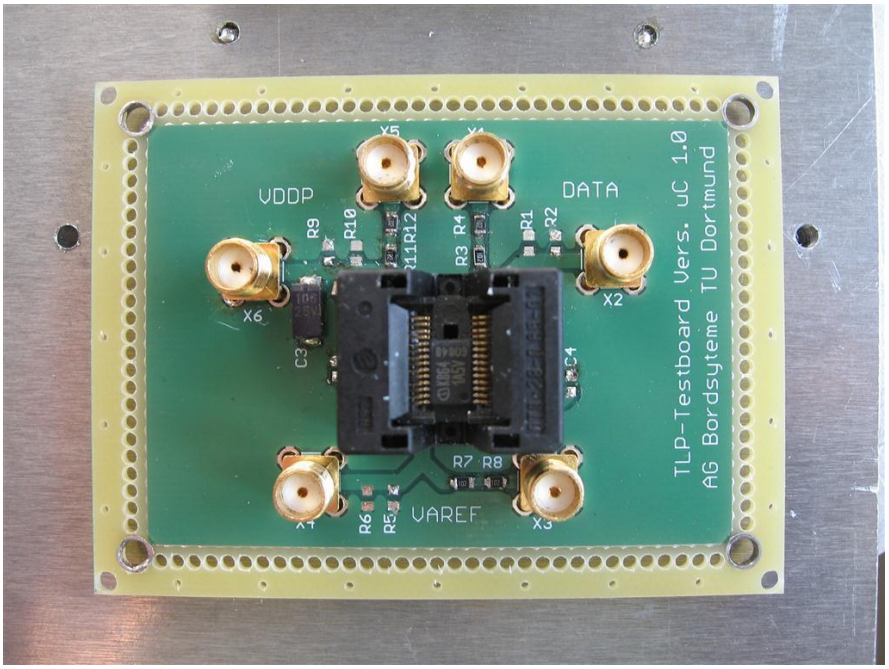

Figure 58: TLP board with µC socket

The settings of the TLP measurement setup are calibrated using a resistor. In Figure 59 the IV curves measured with TLP and source meter for a 47 Ω resistor are compared. The curve consists of 2 TLP datasets and 1 dataset from source meter. For low charging voltages of the TLP some deviations may occur because of high attenuation factors. Precise results are obtained for high charging voltages.

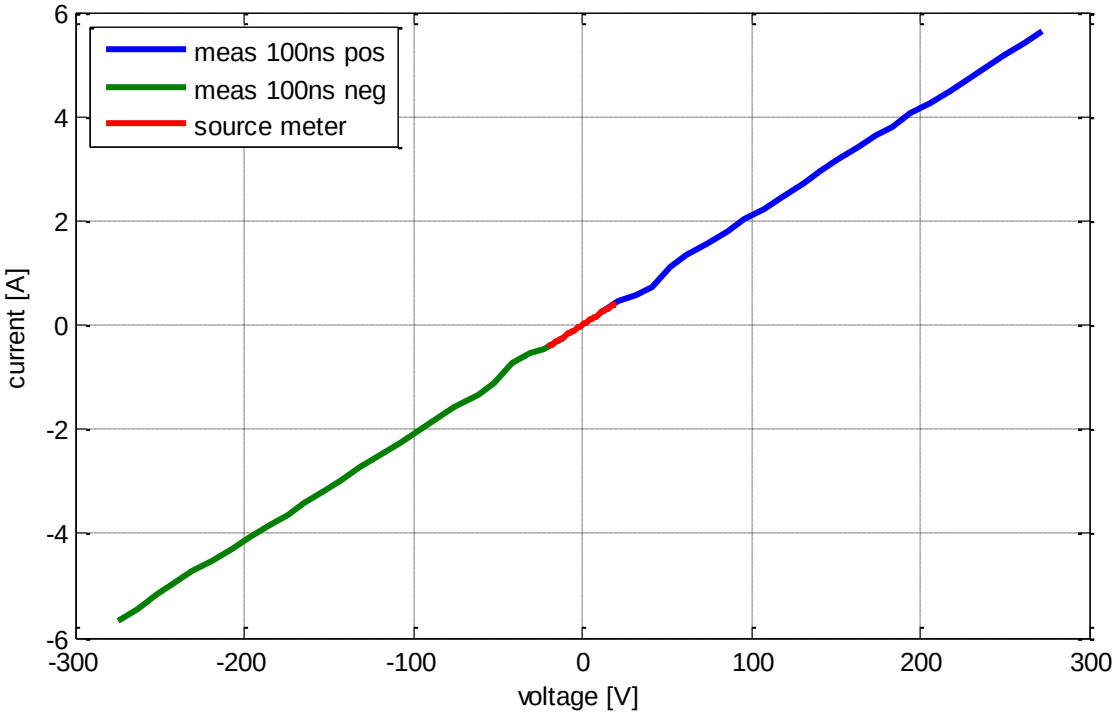

Figure 59: Measured IV curve of a 47 Ω resistor

As a first step for IC testing a TLP sweep with negative and positive charging voltages is done to estimate the negative and positive breakdown voltages of the ESD structures. Then the static behavior is measured with the source meter till 95 % of the estimated breakdown voltage is reached. Breakdown voltage of an IV curve is defined where the current increases more than 10 % compared to the preceding voltage step. From the measured curve a characteristic point is also selected at about 90 % of the defined breakdown voltage. This current at the characteristic point will be monitored after each TLP discharge which is major criteria for destruction of an IC. Permanent IC damage generally is assumed if a DC current measurement at a voltage level before the characteristic point exceeds the initially measured values by a factor of ten.

The failure energies are determined with changing voltage amplitude until destruction of the IC is detected with IV curve measurements. The increment of the charging voltage should be selected dynamically to minimize pre-damaging. Smaller voltage steps are applied close to the level of breakdown voltage which is an first estimation for the failure level.

3.2.2 **Frequency domain measurement setup**

S-parameters are measured with a network analyzer (NWA) according to Figure 60. For more accuracy TLP testboards were used without sockets. The NWA was calibrated by soldering open short and load SMD devices on the PCB close to the IC soldering pads. Values for the pin capacitance C are calculated from S11 parameters at 10 MHz and for pin inductance L at about 1GHz.

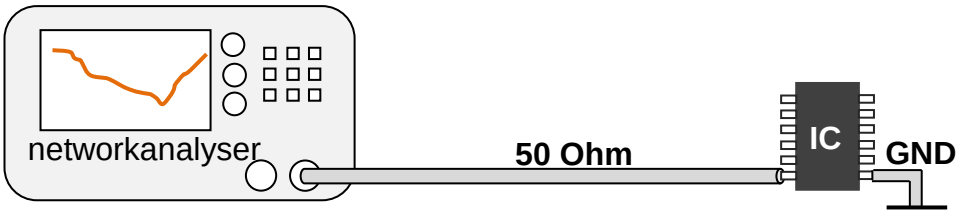

Figure 60: Setup for IC characterization in frequency domain

3.2.3 Characterization of LIN transceiver ATA6662C TxD pin

In Figure 61 the schematic of the measurement setup is shown. 10 µF and 100 nF capacitors are connected to V_S pin in order to obtain realistic conditions for failure model parameter measurements.

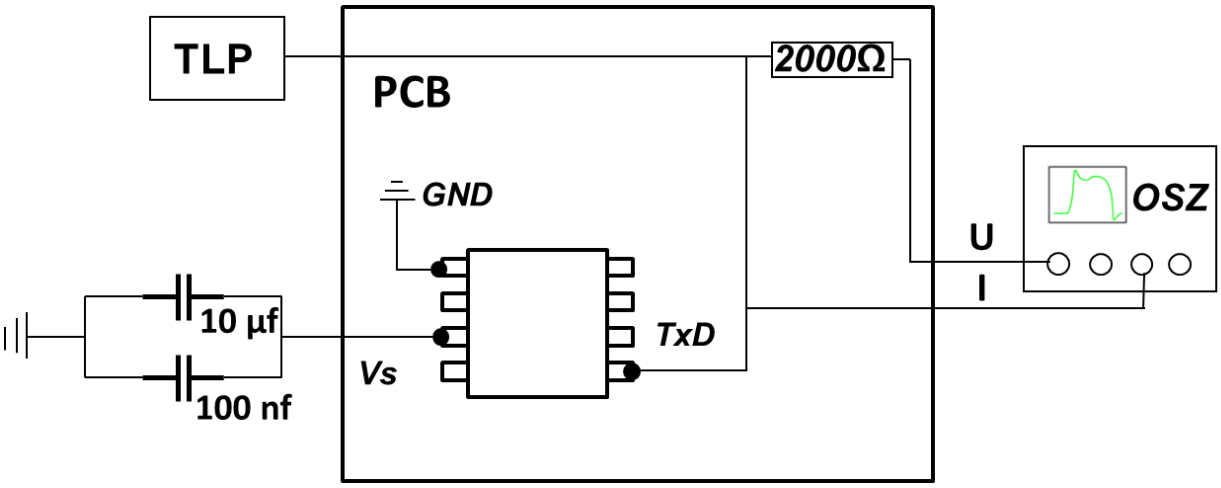

Figure 61: Schematic of TLP measurement setup for LIN ATA6662C TxD pin

The IV curves for the LIN TxD pin are shown in Figure 62. Measurement data up to about 13 A were measured for 25 ns pulse width. Beside from the measured DC spot current yet the last points of each IV curve indicate destruction of the IC because of a significant voltage drop.

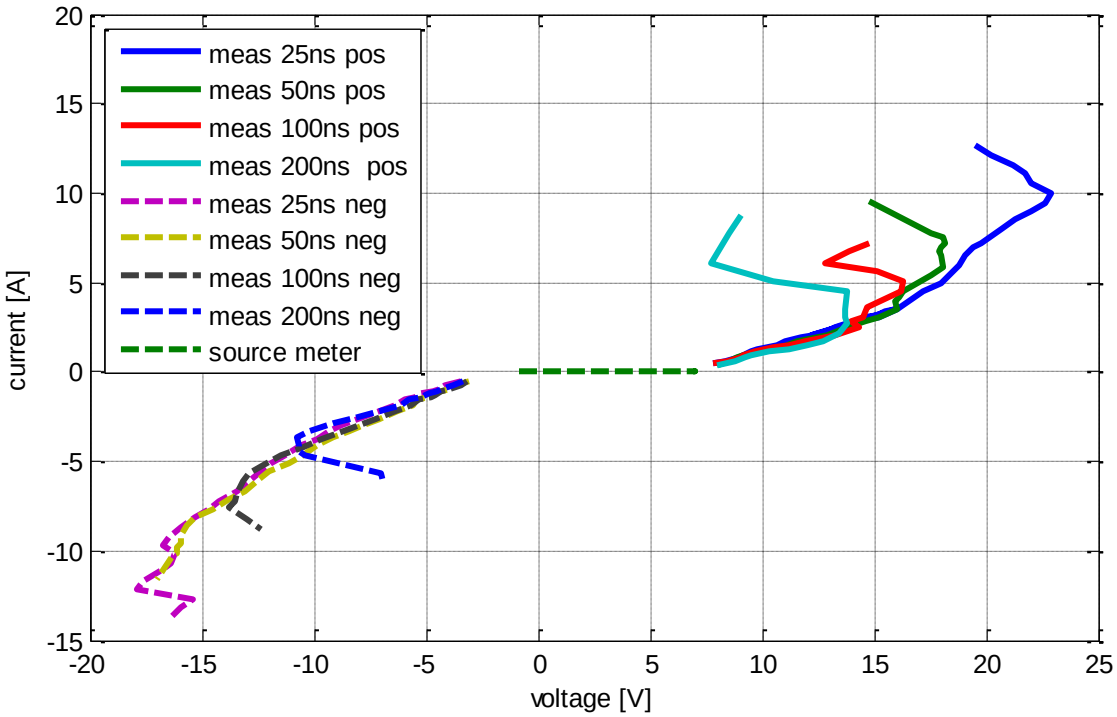

Figure 62: Comparison of measured IV characteristics for LIN TxD pin

In Figure 63 and Figure 64 the critical waveforms are compared for different pulse widths for positive TLP charging voltages before destruction. TLP charging voltage and pulse width behave inversely proportional.

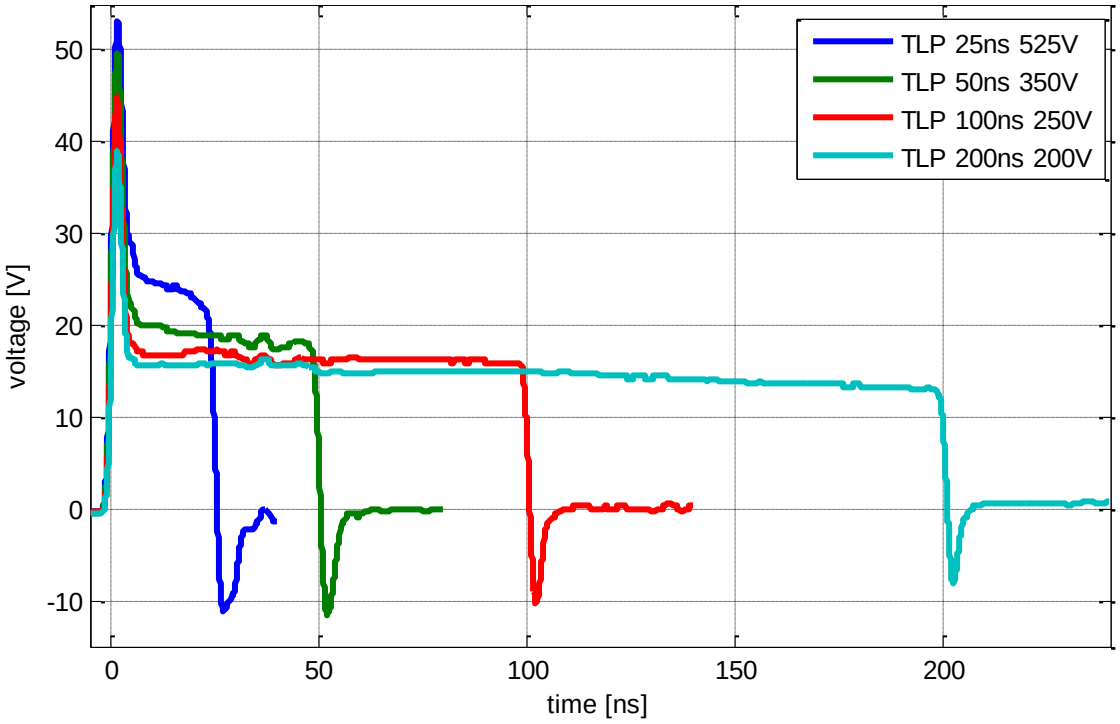

Figure 63: Critical positive voltage waveforms for different pulse widths at LIN TxD pin

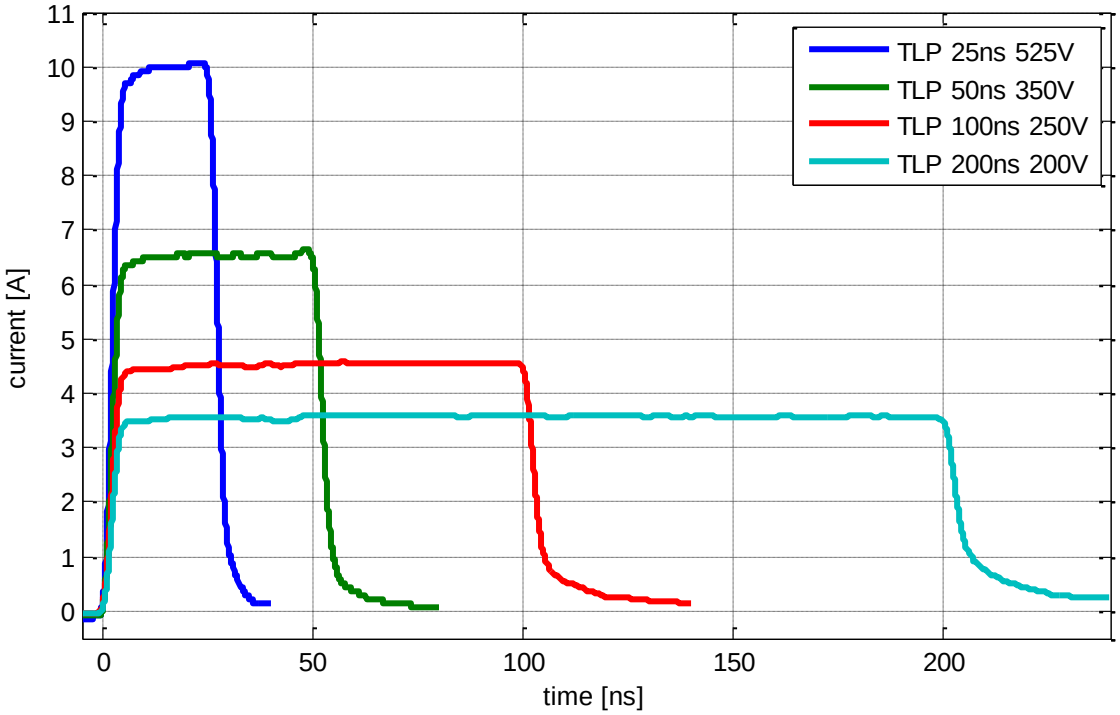

Figure 64: Critical positive current waveforms for different pulse widths at LIN TxD pin

Table 5 summarizes the parameters from the curves. Maximum charging voltage was 525 V where a peak voltage of 53 V and a peak current of 10 A were measured. The energy can be calculated from current and voltage waveforms. For many IC-pins an increasing critical energy can be found with increasing pulse width. This fact can be explained by heat dissipation before the pulse has decayed which is especially true for 200 ns pulses.

IC (PIN)	t_{TLP} [ns]	V_{TLP} [V]	V_{max} [V]	I_{max} [A]	V_{mean} [V]	I_{mean} [A]	E_{crit} [µJ]
LIN-ATA6662C (TXD)	25	525	53.2	10.0	22.9	10	5.8
	50	350	49.7	6.6	18	6.5	6.1
	100	250	44.8	4.6	16.2	4.6	7.4
	200	200	39.0	3.6	13.7	3.6	10.4

Table 5: Measured parameters with variation of TLP pulse width for LIN TxD pin

All parallel IC-capacitances C and serial IC-package-inductances L for modeling were measured with a network analyzer without a bias voltage. Table 6 contains the results for LIN TxD pin. Measurement data in frequency domain was measured without additional capacitors connected to the IC pins.

IC (PIN)	$C_{parallel}$	L_{serial}
TXD	8,5 pF @ 10 MHz	2,5 nH @ 1,1 GHz

Table 6: Measured values L_{serial} and $C_{parallel}$ for LIN TxD pin

3.2.3.1 Verification of LIN model

The measured and the modeled IV curves are compared in Figure 65. For the extension of the model's applicability the IV curve was extrapolated.

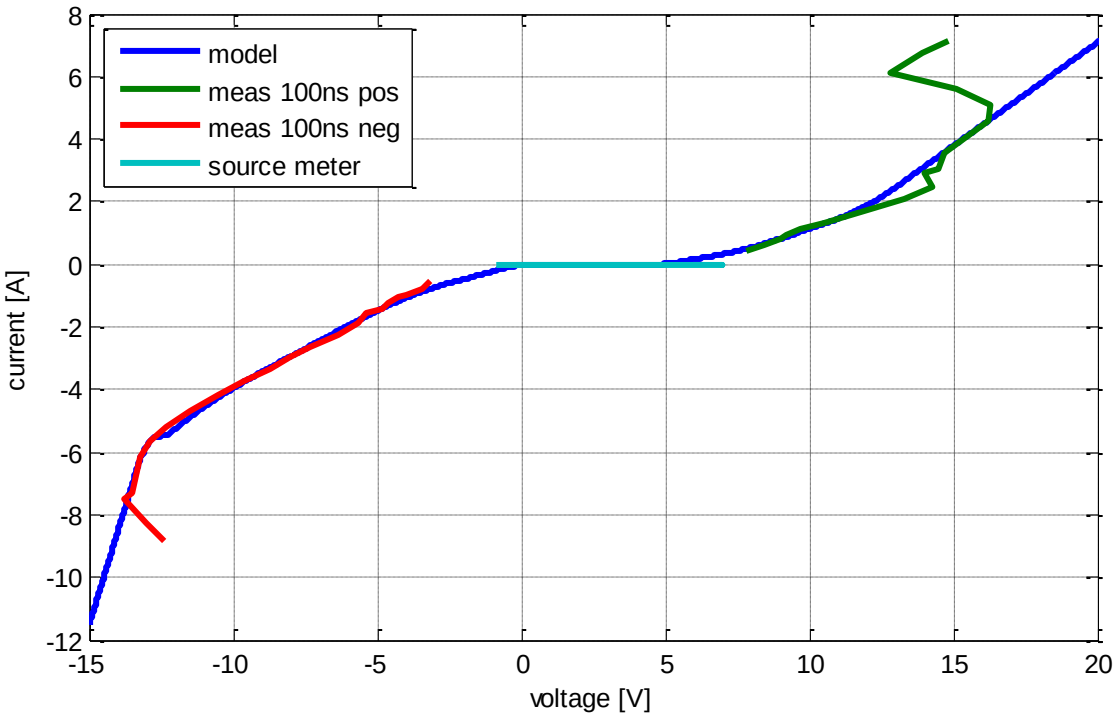

Figure 65: Comparison of measured and simulated IV curves of LIN TxD pin

The model is verified by a comparison of TLP measurement data and simulation of the TLP measurement setup including the IC model. A schematic of the setup is given in Figure 66 for the LIN TxD pin. Beside the TLP model described in section 2.1.4 a 10 nH inductor was added representing the inductance of the socket connected with the TLP testing board in the current return path of the IC.

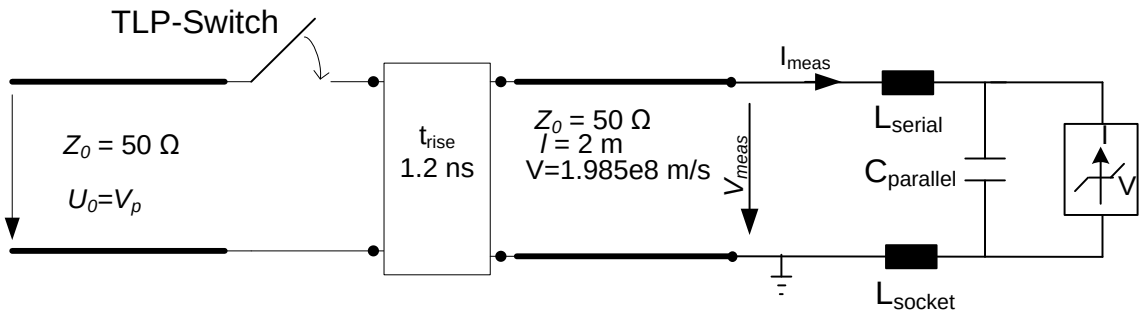

Figure 66: Setup for verification of measured data by simulation

The curves presented in Figure 67 and Figure 68 for 100 ns pulse width show a good matching. The voltage peak is simulated well. For a more accurate modeling of the setup additional parasitic elements should be considered.

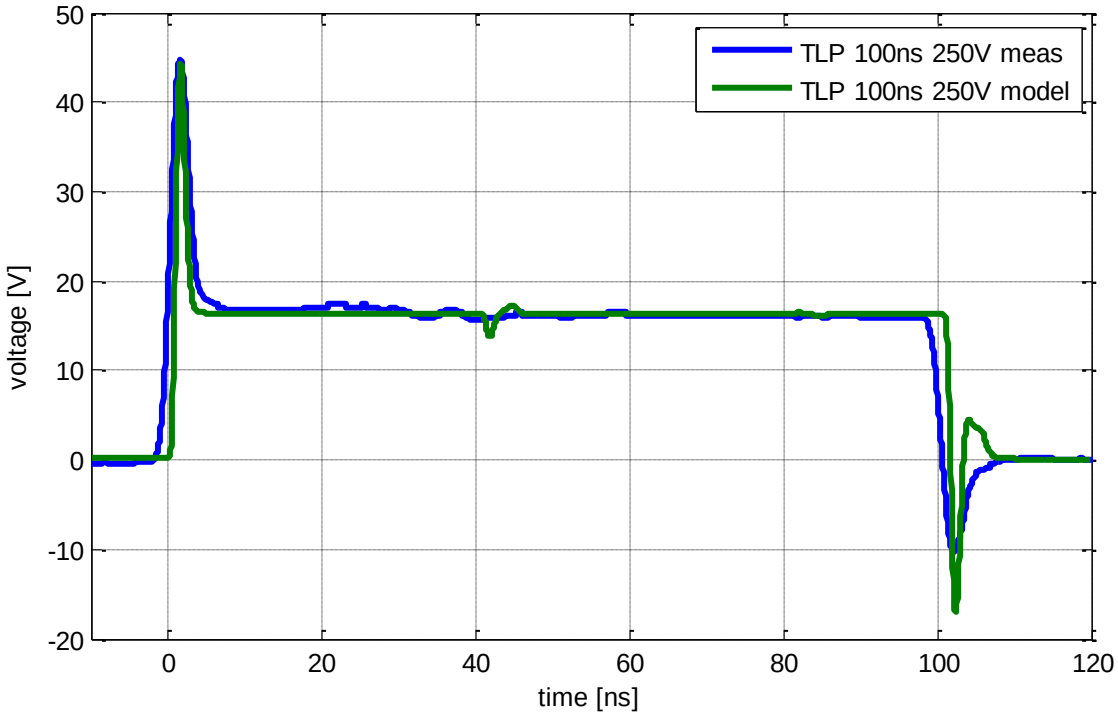

Figure 67: Comparison of measured and simulated voltage at LIN TxD pin

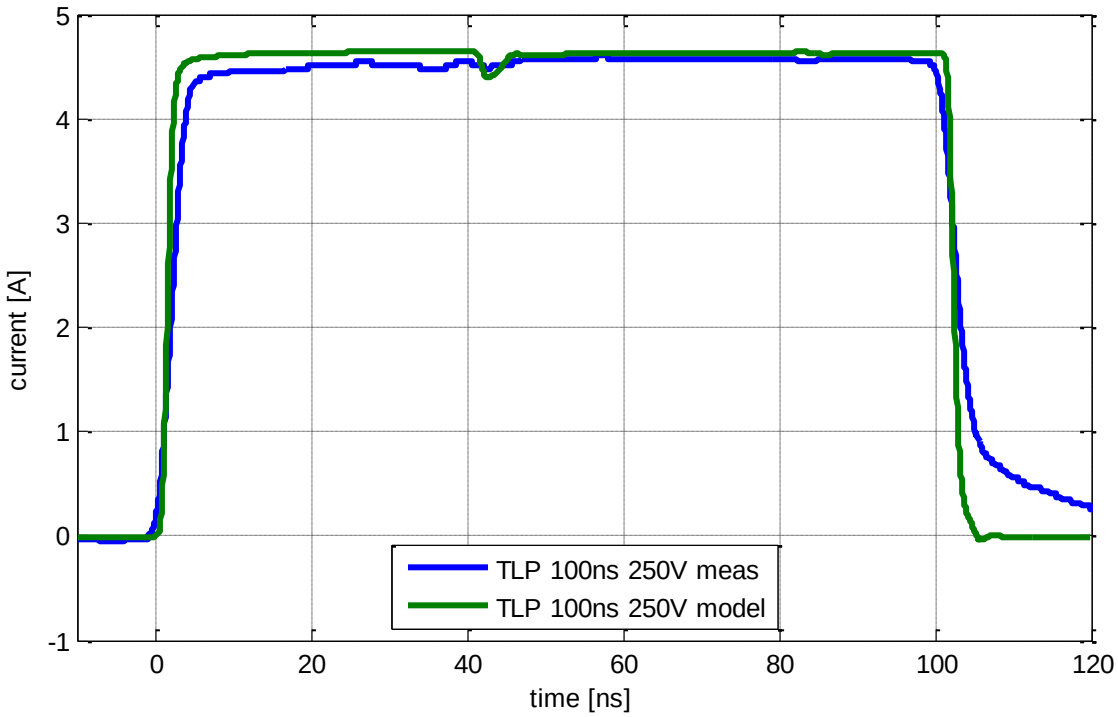

Figure 68: Comparison of measured and simulated current at LIN TxD pin

3.2.4 Characterization of CAN transceiver TJA1041T CANH pin

Similar to the LIN transceiver 10 µF and 100 nF capacitors were connected to the Vs and Vcc pin during TLP measurement. A circuit diagram is given in Figure 69.

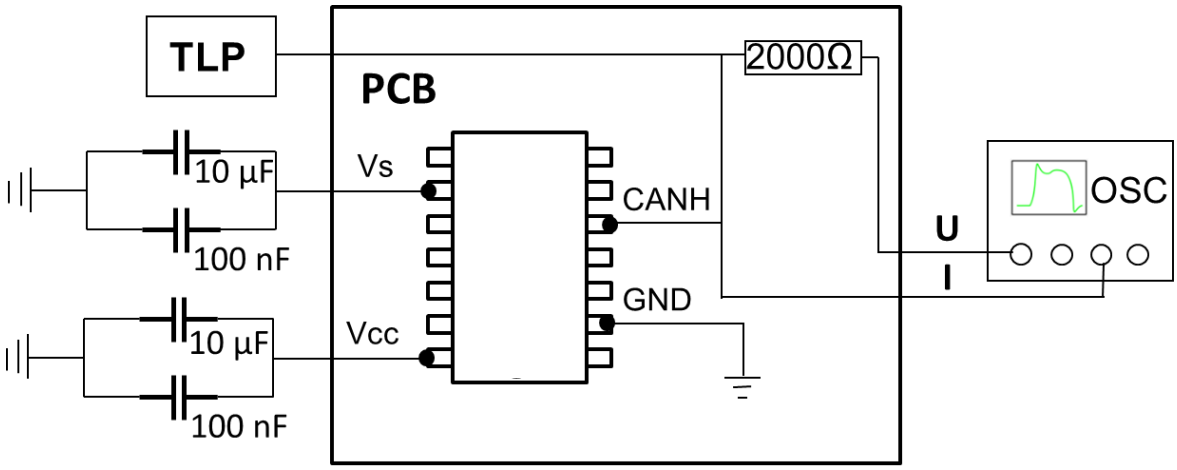

Figure 69: Circuit diagram of TLP measurement setup for CAN TJA1041T CANH pin

The overlaying IV curves of the selected CANH pin are shown in Figure 70 for positive charging voltages. Destruction was detected for all pulse widths.

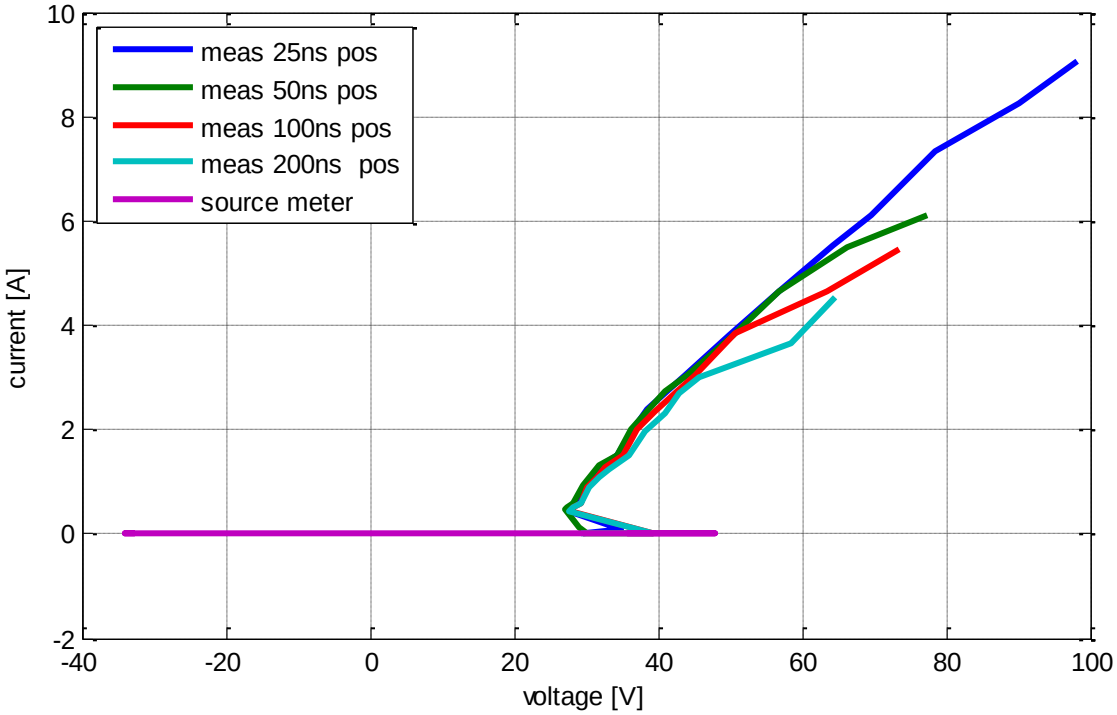

Figure 70: Comparison of measured IV-characteristics for CANH pin

The positive critical curve shapes of TLP pulses for the CANH pin are shown in Figure 71 and in Figure 72. Table 7 includes all measured amplitudes and energies for the selected pulse widths. The highest amplitudes before destruction is detected is about 126 V and 7,3 A. Similar to LIN TxD the calculated energies differ by a factor of 2 for 25 ns and 200 ns pulses.

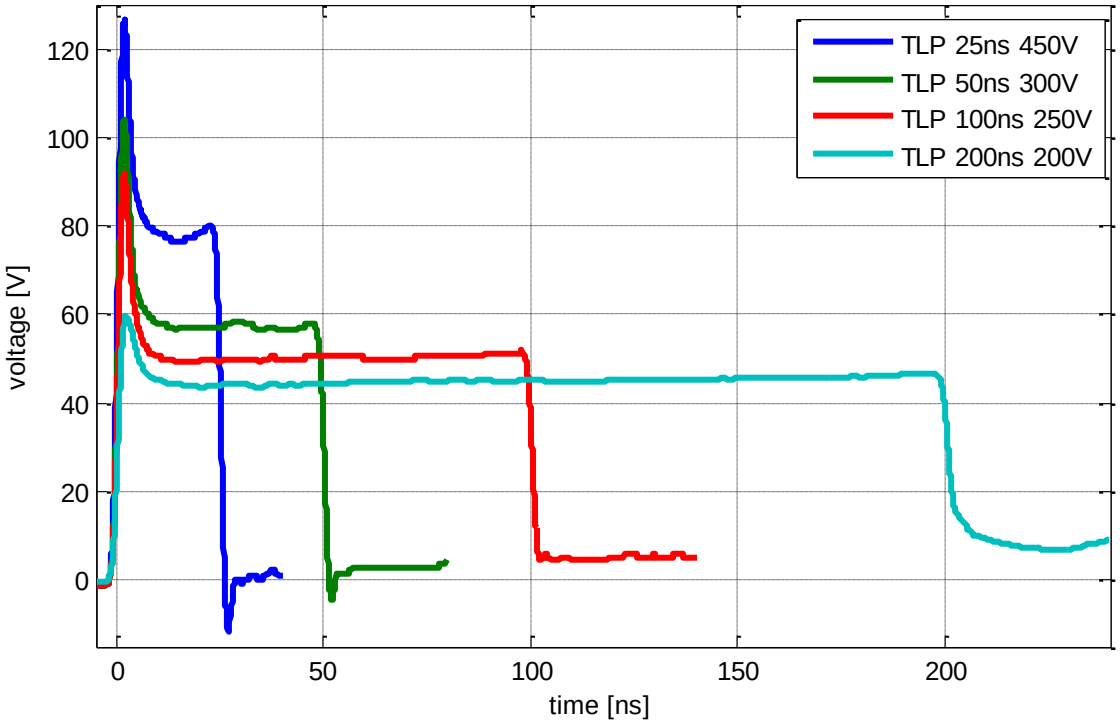

Figure 71: Critical positive voltage waveforms for different pulse widths at CANH pin

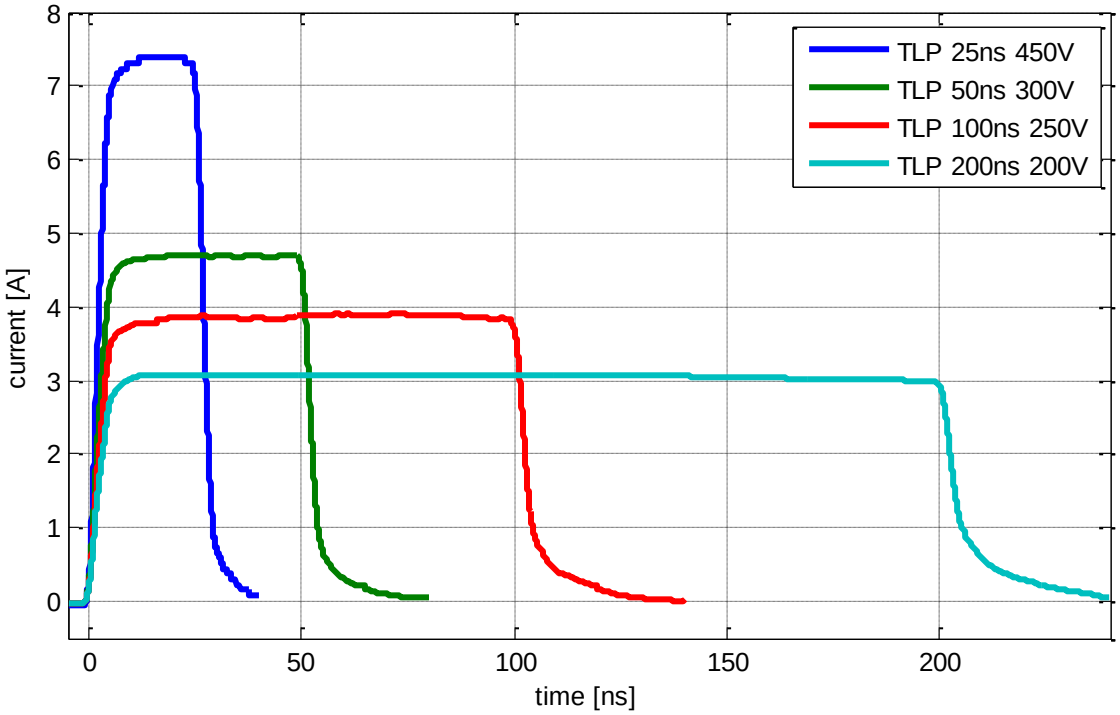

Figure 72: Critical positive current waveforms for different pulse widths at CANH pin

IC (PIN)	t_{TLP} [ns]	V_{TLP} [V]	V_{max} [V]	I_{max} [A]	V_{mean} [V]	I_{mean} [A]	E_{crit} [µJ]
CAN-TJA1041T (CANH)	25	450	126.5	7.3	78.5	7.3	13.6
	50	300	104.1	4.7	56.7	4.6	13.1
	100	250	91.8	3.9	50.6	3.9	19.2
	200	200	59.5	3.0	45.7	3	27.5

Table 7: Measured parameters with variation of TLP pulse width for CANH pin

In frequency domain a capacitance of 10,5 pF and inductance of 4,5 nH was measured for the CANH pin.

IC (PIN)	$C_{parallel}$	L_{serial}
CANH	10,5 pF @ 10 MHz	4,5 nH @ 1 GHz

Table 8: Measured values for L_{serial} and $C_{parallel}$ for CANH pin

3.2.4.1 Verification of CAN model

In Figure 73 measurement results and a simulated IV curve of the CANH pin are compared. Good matching can be obtained for positive and negative TLP charging voltages. The corresponding TLP simulation for 100 ns pulse width can be found in Figure 74 and Figure 75. L_{socket} was set to 18 nH.

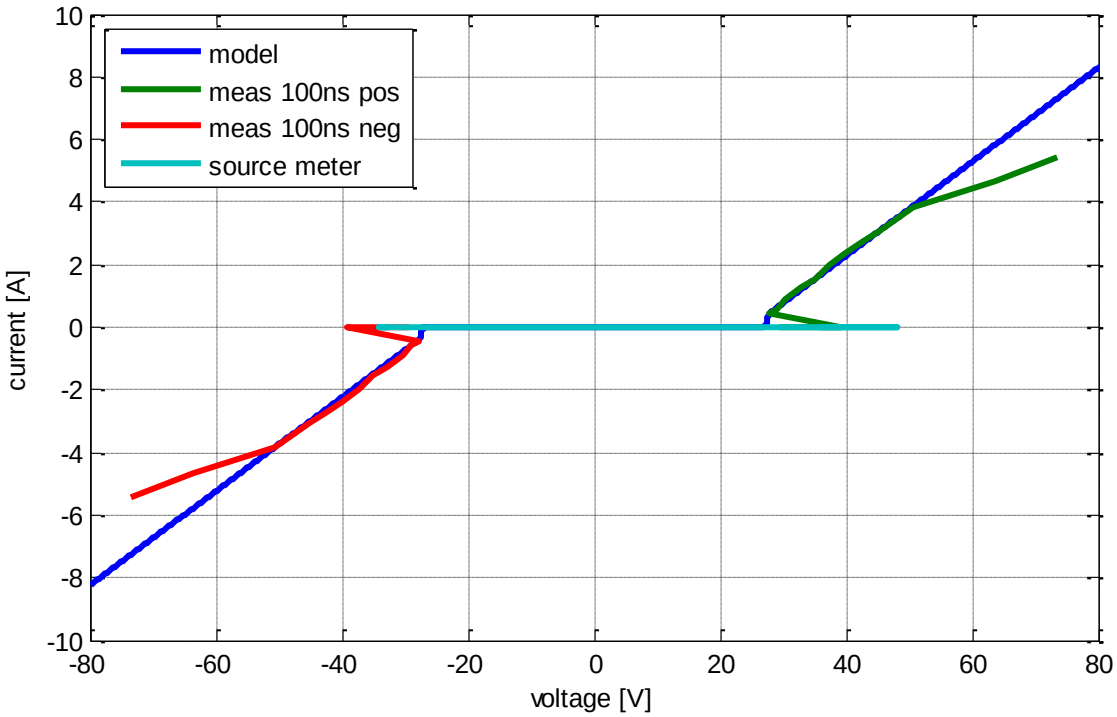

Figure 73: Comparison of measured and implemented IV-curves of CANH pin

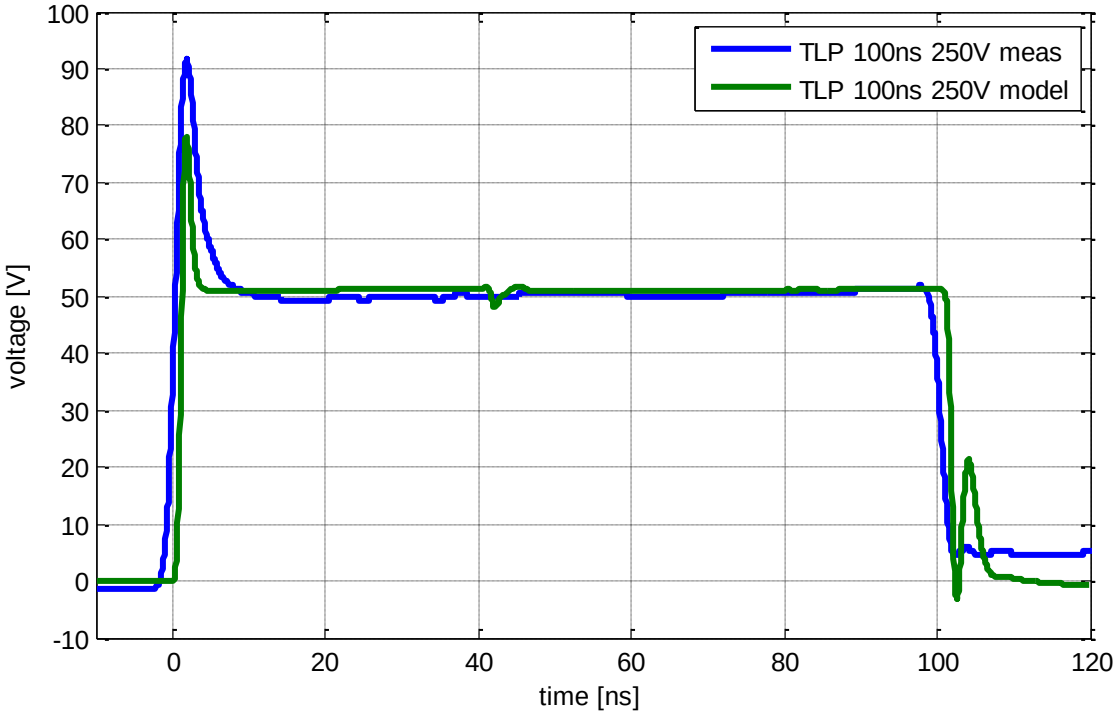

Figure 74: Comparison of simulated and measured voltage for positive TLP charging voltage at CANH pin

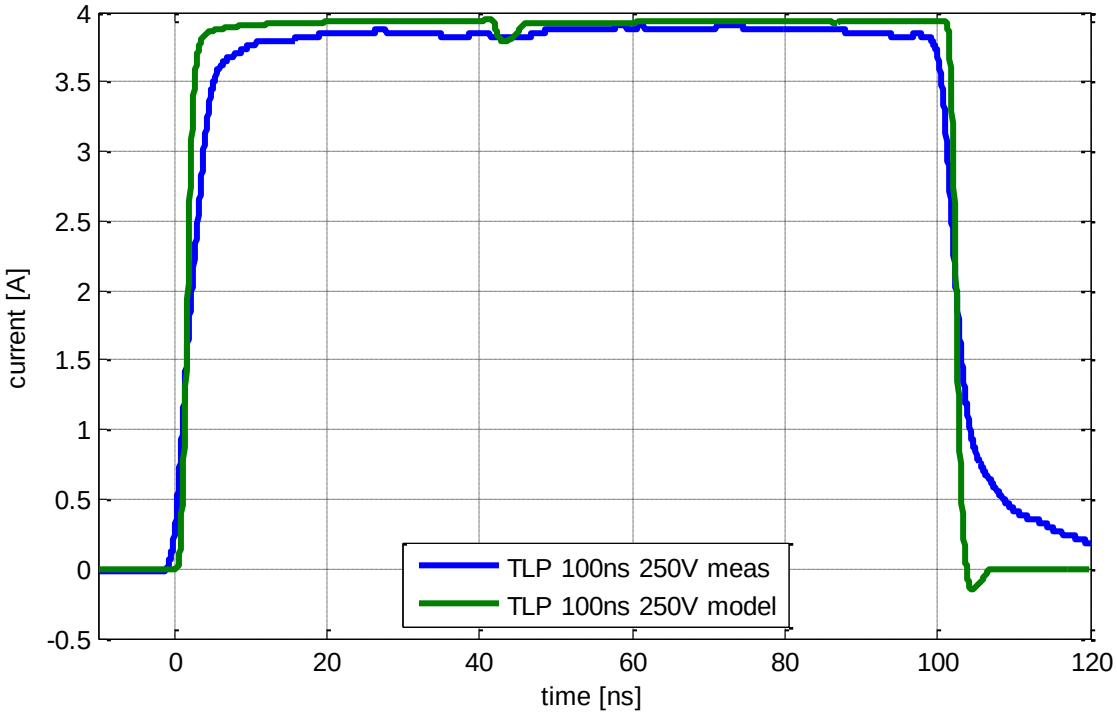

Figure 75: Comparison of simulated and measured current for positive TLP charging voltage at CANH pin

3.2.5 Characterization of µC XC864 DATA pin

Characterization and modeling results are described for the DATA pin of the XC864 microcontroller in this section. 10 µF and 100 nF capacitors were soldered in parallel to the VDDP pin during the TLP test as shown in Figure 76.

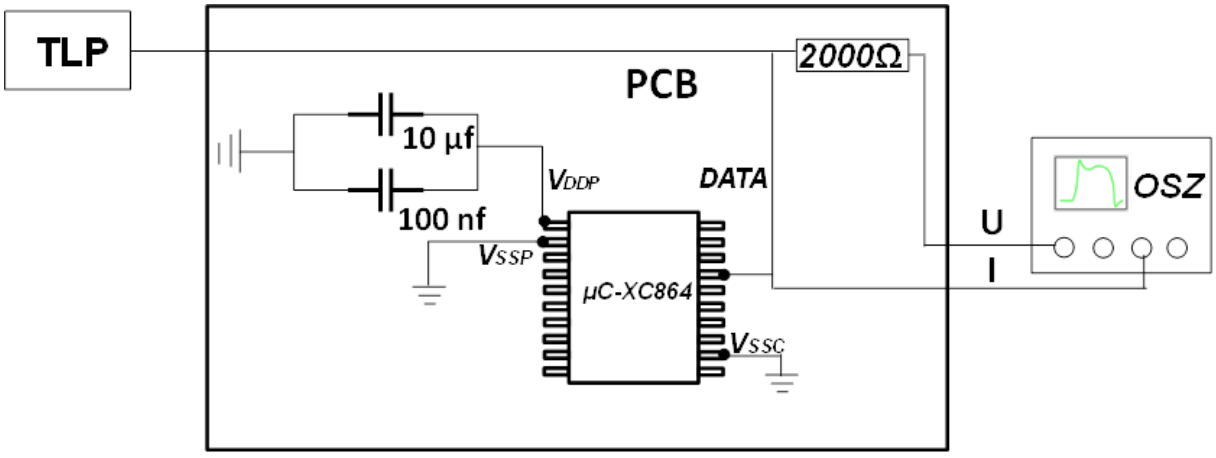

Figure 76: Circuit diagram of TLP measurement setup for XC864 DATA pin

Measured IV curves of the DATA pin are compared in Figure 77. The pin turns out to be fail at current amplitudes of less than minus 20 A. In comparison to the characteristic of CAN and LIN transceiver pins the failure voltage of the DATA pin is quite low.

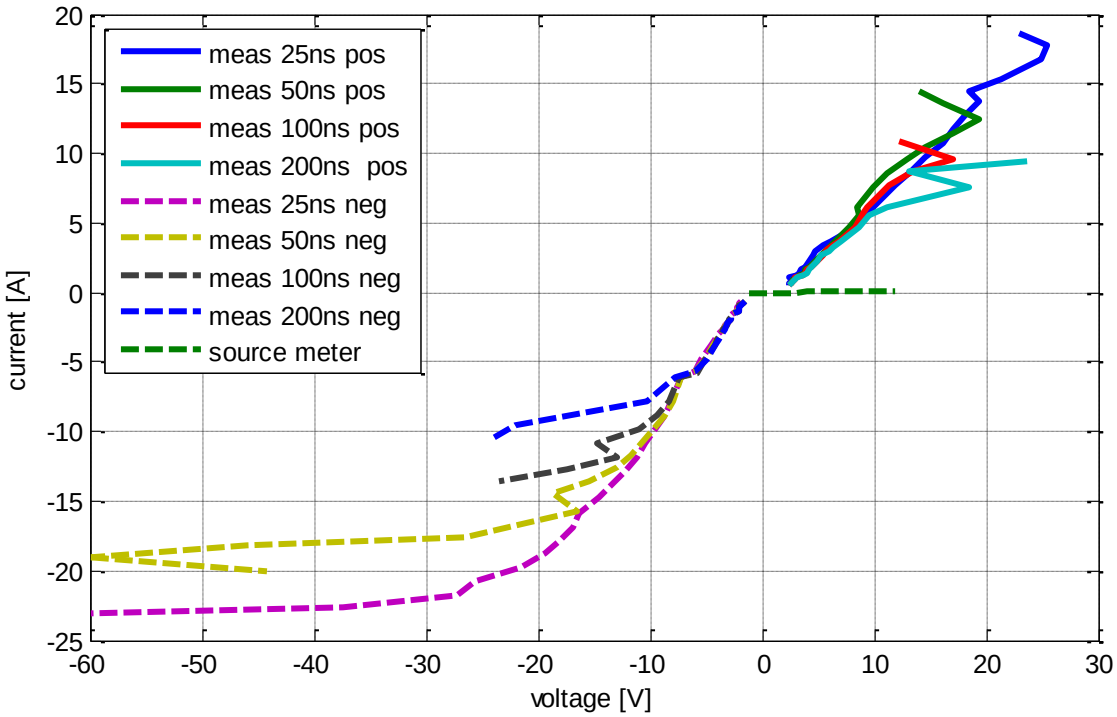

Figure 77: Comparison of measured IV-characteristics for DATA pin of µC

In the plots comparing critical voltage over pulse width for positive TLP charging voltages the clamping voltage of all curves is about 20 V. In Figure 78 a slight rise of the voltage can be observed with progress of the TLP pulse. This could be caused by heating effects in the current path of the IC.

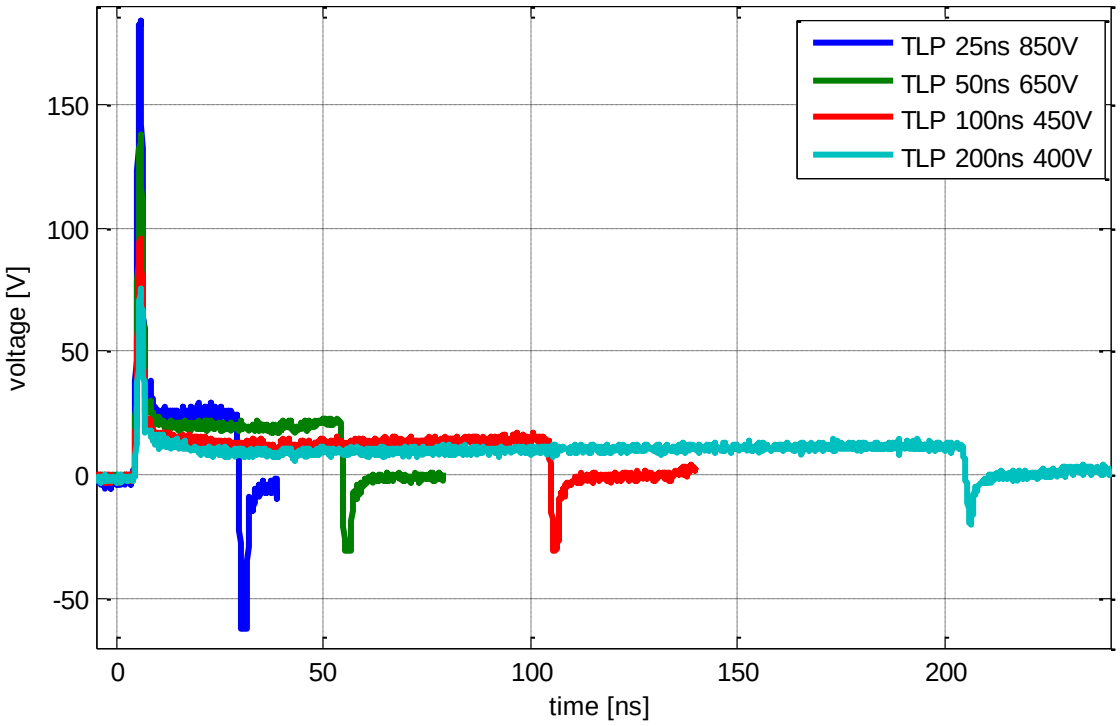

Figure 78: Critical positive voltage waveforms for different pulse widths at DATA pin of XC864

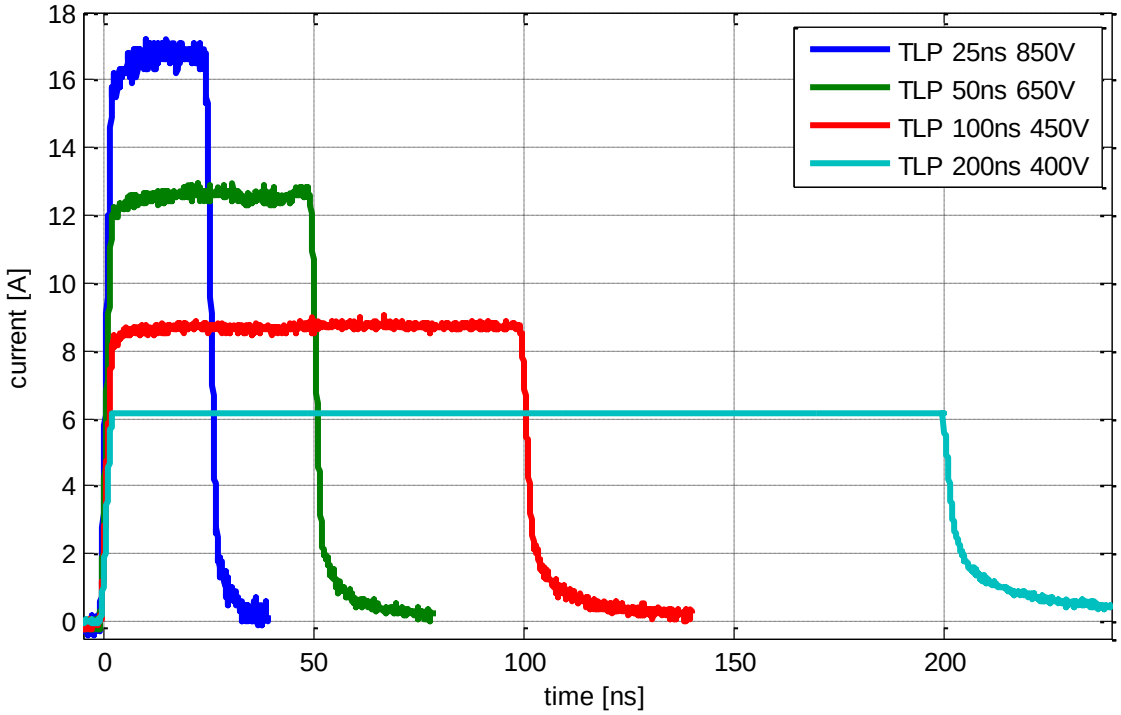

Figure 79: Critical positive current waveforms for different pulse widths at DATA pin of XC864

The maximum TLP charging voltage before destruction was 850 V. The highest voltage and current amplitudes of all tested ICs are reached at about 183 V and 17 A. The calculated critical energy from the pulses was found to be very stable.

IC (PIN)	t_{TLP} [ns]	V_{TLP} [V]	V_{max} [V]	I_{max} [A]	V_{mean} [V]	I_{mean} [A]	E_{crit} [µJ]
µC-XC864 (DATA)	25	850	183.7	17.2	24.9	16.7	12.7
	50	650	138.1	12.9	19.3	12.5	13.9
	100	450	95.4	9.0	13.5	8.7	12.3
	200	400	75.2	6.1	11.1	6.1	13.3

Table 9: Measured parameters with variation of TLP pulse width for µC DATA pin

$C_{parallel}$ and $L_{parallel}$ are set to 7,6 pF and 9,2 nH in the model.

IC (PIN)	$C_{parallel}$	L_{serial}
µC_XC864(DATA)	7,6 pF @ 10 MHz	9,2 nH @ 1,2 GHz

Table 10: Measured values L_{serial} and $C_{parallel}$ for XC864 µC

3.2.5.1 Verification of µC model

In Figure 80 the simulated and measured IV characteristics are compared for 100 ns pulse width.

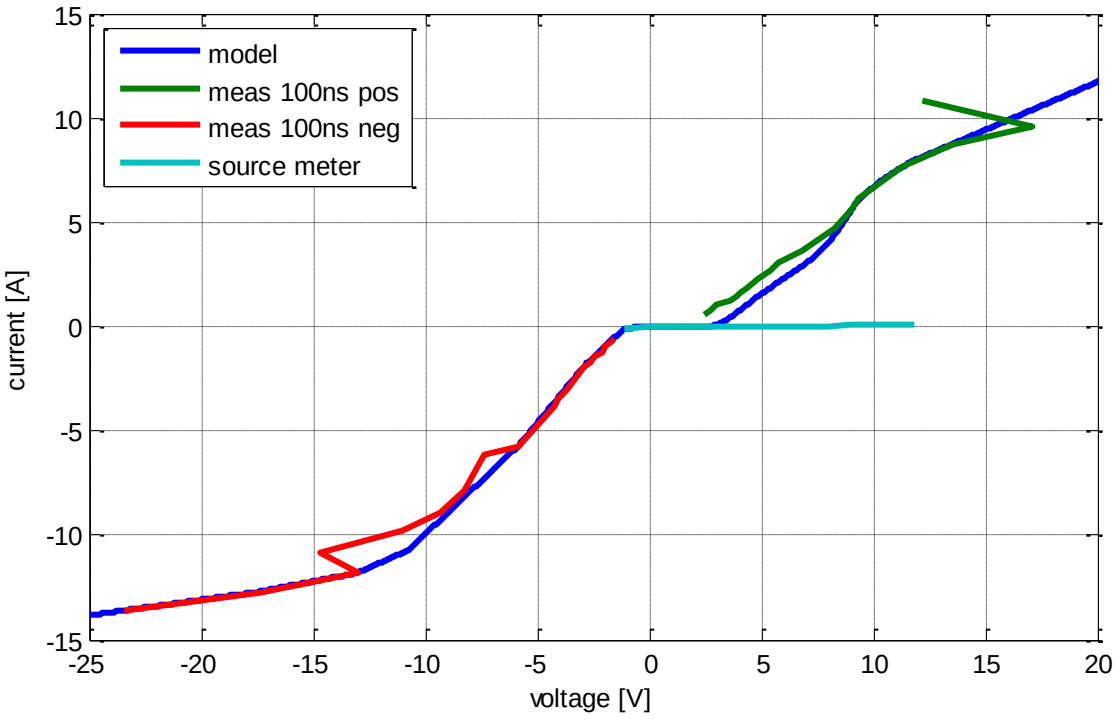

Figure 80: Comparison of measured and implemented IV-curves of µC DATA pin

A good matching was obtained comparing simulation and measurement data in Figure 81 and Figure 82. L_{socket} was set to 18 nH.

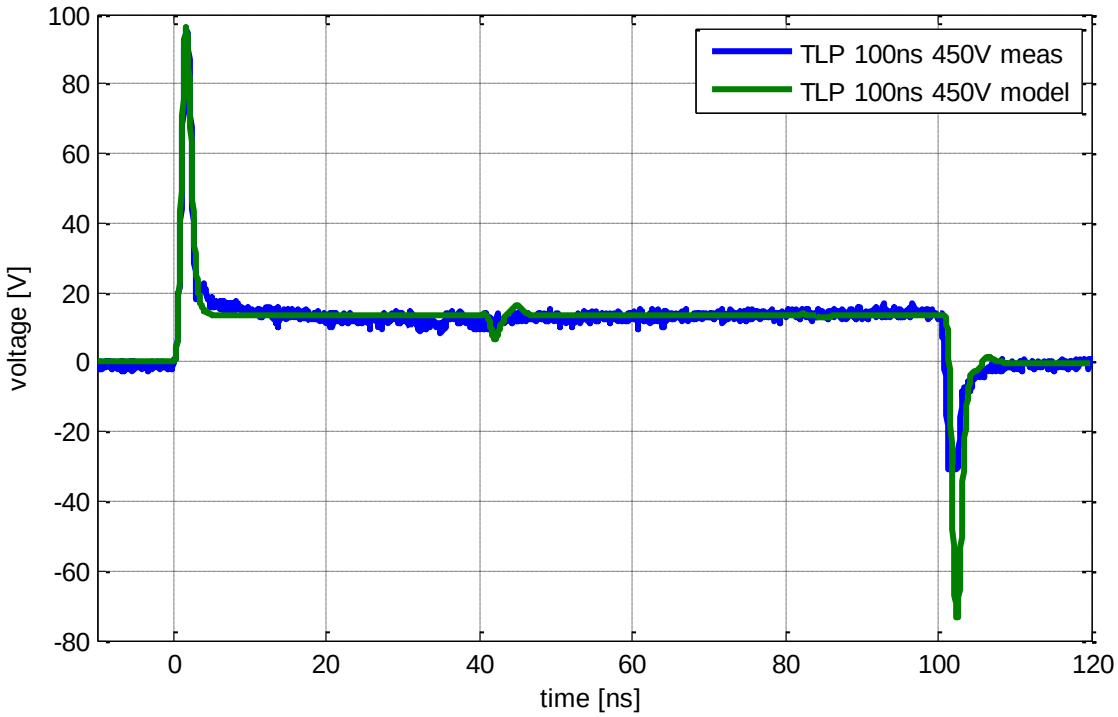

Figure 81: Comparison of simulated and measured voltage for positive TLP charging voltage at DATA pin of XC864 µC

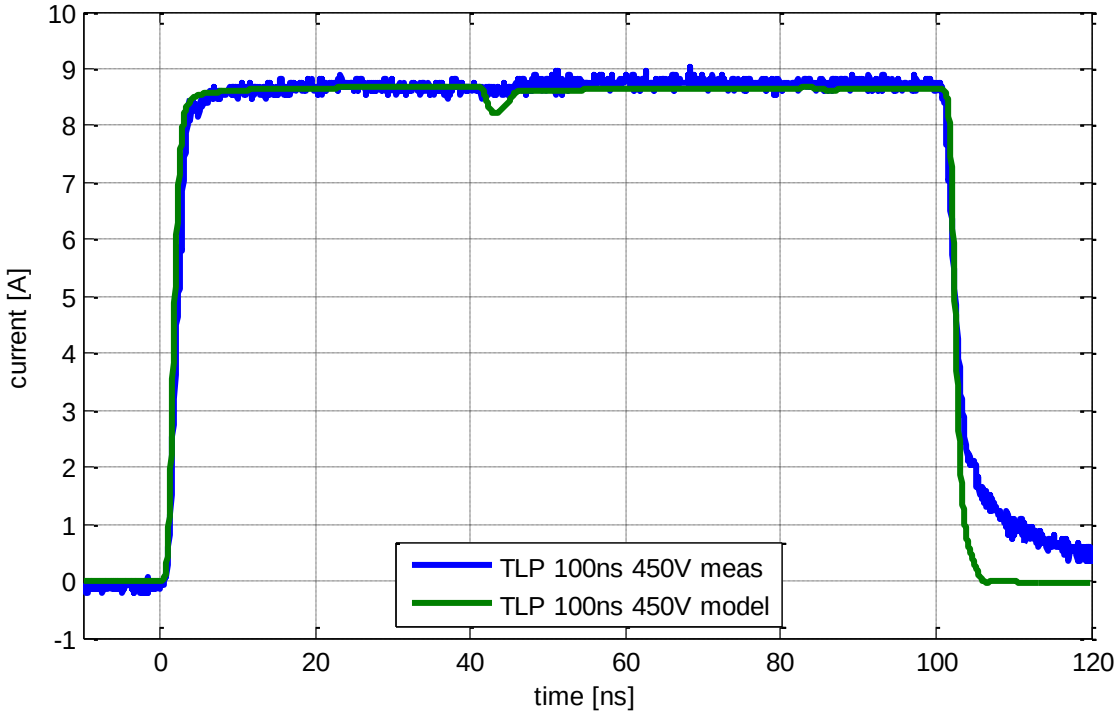

Figure 82: Comparison of simulated and measured current for positive TLP charging voltage at DATA pin of XC864 µC

3.3 ICs with lower ESD robustness

The impact of ESD coupling on ICs with lower ESD robustness is investigated based on simulation. The ESD robustness of the models presented and verified in section 3.2 is modified according to the method described in section 2.3.3. The scaling method is based on the concept of a critical energy when IC pins might be destroyed.

The calculated failure energies at the IC pin causes a temperature rise up to critical values.

3.3.1 **IEC robustness factor 0,5**

In Table 11 the failue energies and necessary charging voltages of an IEC ESD generator are shown. The voltage for which the critical temperature can be calculated was simulated using the IC model described in section 3.2. A new critical energy was simulated by setting half of the charging voltage of the measured value. Because the temperature rise is sensitive to small changes of the values a deviation of some degrees K has to be accepted. Because of the resistive IV characteristic of the ICs the scaling factor corresponding to the failure energy usually is different from the factor used for the charging voltage.

IC	IEC-failure simulation [kV]		failure energy [µJ]		failure temperature [K]	
	reference	IEC/2	reference	IEC/2	reference	IEC/2
µC-XC864 (DATA)	4,55	2,27	13	3,8 (3,42)	1711	1709
LIN-ATA662C (TXD)	3,0	1,5	8,1	2,91 (2,78)	1695	1687
CAN-TJA1041T (CANH)	2,9	1,45	22,19	8,09 (2,74)	1704	1701

Table 11: Calculated factors for IEC/2 ESD robustness scaling

The minimal failure energy is 2,91 µJ and was calculated for the LIN transceiver. A bisection of the IEC ESD robustness voltage results in a scaling factor of about 3 for the energy. The corresponding values for the thermal capacitance C_{th} and resistance R_{th} are summarized in Table 12. Because the ESD robustness is reduced, C_{th} has to be reduced too. The active area inside the semiconductor is getting smaller which causes increasing thermal resistance because heat dissipation depends on surface effects.

IC	therm. capacitance [nJ/K]		therm. resistance [K/W]	
	reference	IEC/2	reference	IEC/2
µC-XC864 (DATA)	8.87	2.59	730	2497
LIN-ATA662C (TXD)	5.37	1.93	470	1308
CAN-TJA1041T (CANH)	13.9	5.07	91	249

Table 12: Thermal capacitance and resistance for IC pins with IEC/2 ESD robustness

3.3.2 **HBM robustness factor 0,5**

In Table 13 and Table 14 all parameters are given for a bisection of the HBM robustness. The reference values were simulated using the HBM model described in section 2.1.1. Similar scaling factors were calculated as for the IEC generator.

IC	HBM-failure simulation [kV]		failure energy [µJ]		failure temperature [K]	
	reference	HBM/2	reference	HBM/2 (factor)	reference	HBM/2
µC-XC864 (DATA)	11,45	5,725	13,27	4,04 (3,29)	1687	1678
LIN-ATA662C (TXD)	7,0	3,5	8,7	3,46 (2,52)	1689	1682
CAN-TJA1041T (CANH)	6,4	3,2	24,6	9,6 (2,56)	1685	1690

Table 13: Calculated factors for HBM/2 ESD robustness scaling

IC	therm. capacitance [nJ/K]		therm. resistance [K/W]	
	reference	HBM/2	reference	HBM/2
µC-XC864 (DATA)	8,87	2,7	730	2400
LIN-ATA662C (TXD)	5,37	2,13	470	1185
CAN-TJA1041T (CANH)	13,9	5,41	91	233

Table 14: Thermal capacitance and resistance for IC pins with HBM/2 ESD robustness

3.3.3 **HBM 2 kV and 1 kV robustness**

The lowest critical energies are obtained with models scaled to 2 kV and 1 kV HBM charging voltage. All scaling parameters are compared in Table 15 and Table 16. The maximum scaling factor is obtained for the 2 kV HBM model of the µC DATA pin. Scaling factors of CAN and LIN models are similar. Critical energies remain different

for all models. The lowest critical energy is obtained in case of the µC scaled to 1 kV HBM level. Melting temperature is reached for a calculated energy of about 350 nJ. The active area in the semiconductor decreases so that a high thermal resistance is expected.

IC	failure energy [µJ]			failure temperature [K]		
	ref.	2 kV (factor-orig.)	1 kV (factor-2kV)	ref.	2 kV	1 kV
µC-XC864 (DATA)	13,27	0,82 (16,14)	0,35 (2,54)	1687	1671	1670
LIN-ATA662C (TXD)	8,7	1,66 (5,24)	0,69 (2,40)	1689	1675	1670
CAN-TJA1041T (CANH)	24,6	5,18 (4,74)	2,07 (2,51)	1685	1689	1683

Table 15: Failure energies for HBM 2 kV and 1 kV scaled IC inputs

IC	therm. capacitance [nJ/K]			therm. resistance [K/W]		
	reference	2 kV	1 kV	reference	2 kV	1 kV
µC-XC864 (DATA)	8,87	0,55	0,23	730	11785	27917
LIN-ATA662C (TxD)	5,37	1,025	0,42	470	2463	5919
CAN-TJA1041T (CANH)	13,9	2,93	1,17	91	432	1082

Table 16: Calculated values for HBM 2 kV and 1 kV scaled IC inputs

3.3.4 **Comparison of scaling Results**

The simulated ESD robustness of all IC models is compared in terms of the critical charging voltage of IEC ESD generator and HBM generator. According to Table 17 HBM charging voltage is more than factor 2 higher than IEC charging voltage for scaled and reference models.

IC (pin)	Failure Levels					
	Reference model		2 kV HBM (scaled model)		1 kV HBM (scaled model)	
	HBM failure voltage [kV]	IEC failure voltage [kV]	HBM failure voltage [kV]	IEC failure voltage [kV]	HBM failure voltage [kV]	IEC failure voltage [kV]
µC-XC864 (DATA)	11,45	5,5	2	1,05	1	0,55
LIN-ATA662C (TXD)	7,0	3,0	2	0,9	1	0,5
CAN-TJA1041T (CANH)	6,4	2,5	2	0,9	1	0,45

Table 17: Comparison of HBM and IEC ESD robustness of reference and scaled IC models

4 Measurement results

In this chapter system level measurement and simulation data are compared to verify the simulation based approach. The demonstrator PCB design is used to build up several measurement setups.

First the parameterization of the VHDL-AMS multi conductor transmission line model is verified in frequency domain. In Section 4.2 signals from IEC generator and TLP discharges are measured for two load conditions. In Section 4.3 a protection element was connected to a PCB trace (transmission line-TL). The simulated IEC robustness of the IC models is verified on the demonstrator PCB in section 4.4. The function of selected protection elements is also verified here. Results presented in section 4.5 were measured for the loop section on the demonstrator PCB.

4.1 Coupling between striplines in frequency domain

In section 2.2 the multi conductor transmission line model was verified by comparison to a highly accurate 3D simulation. The parameterization of the model has to be adapted to the structures on the demonstrator PCB. Values for common and differential mode impedances are calculated using theoretical equations for stripline configurations which are implemented in the freeware tool [16]. For the investigations a coupled multi stripline configuration over a ground plane is selected.

4.1.1 **Setup**

The impedances Z_{even} and Z_{odd} can be calculated with TXLINE tool for given geometry values and material parameters. It is assumed that the transmission line parameters are frequency independent. In Figure 83 and Figure 84 the parameters extracted from the PCB design presented in chapter 1 are used. The relative permittivity ε_r was set to 4,55.

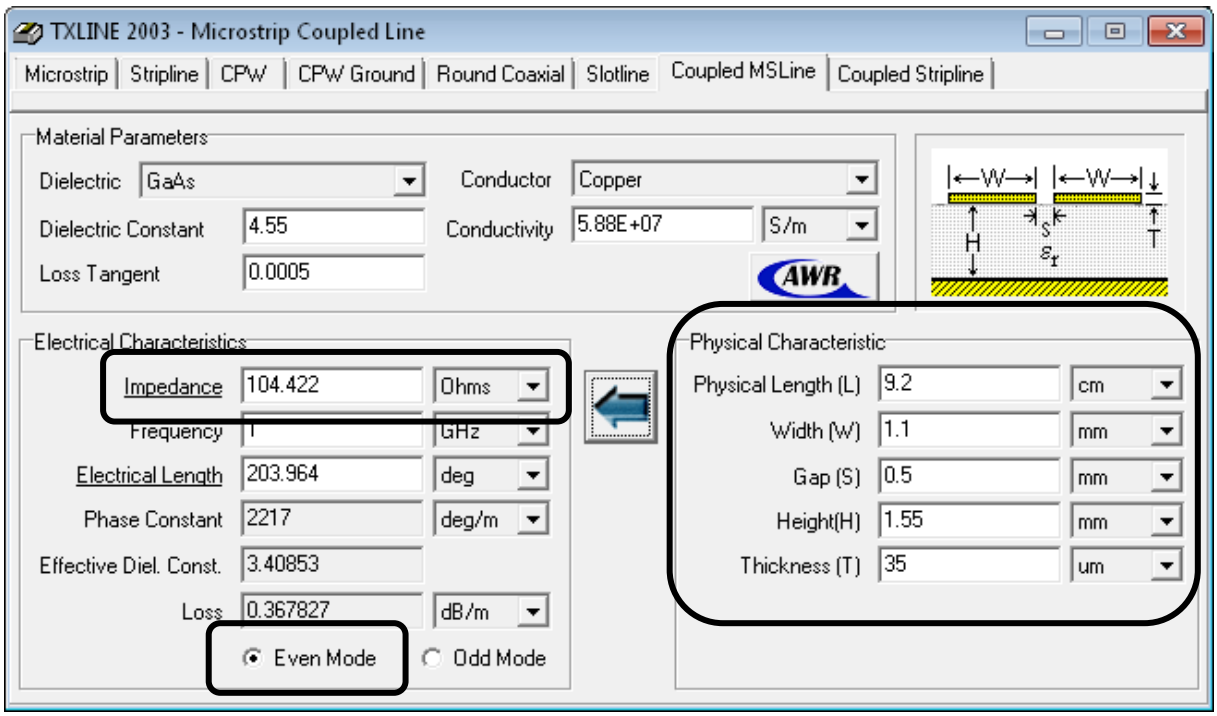

Figure 83: Parameter set for VHDL-AMS model in Even Mode

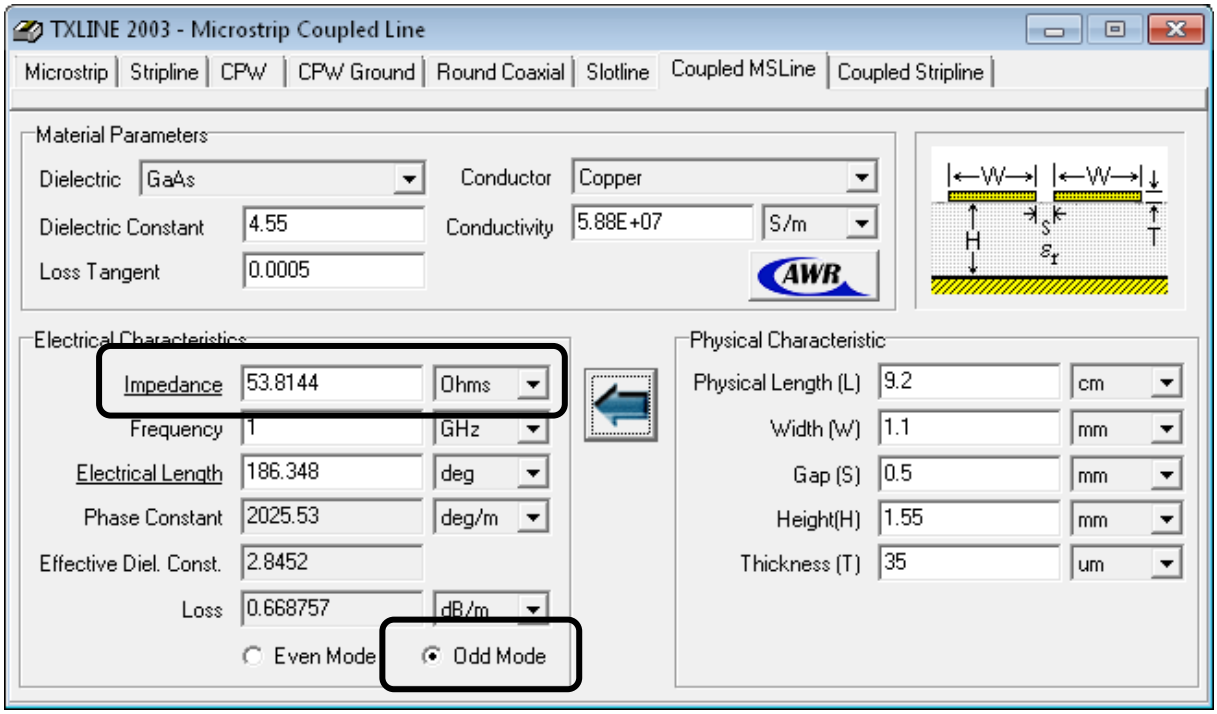

Figure 84: Parameter set for VHDL-AMS model in Odd Mode

For verification of the parameter set S-parameters were measured from the crosstalk section on the demonstrator PCB with a network analyzer. A sketch of the measurement setup is shown in Figure 85. Both transmission lines are terminated with 51 Ω at nodes N3 and N1 and with the 50 Ω source impedance at nodes N2 and N4. The bandwidth was 300 kHz to 1,2 GHz.

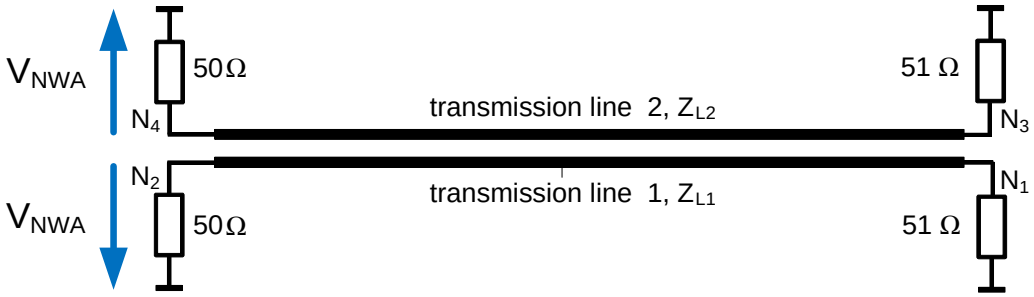

Figure 85: Measurement setup with network analyzer

4.1.2 Comparison with simulation and verification of the transmission line model

The measurement setup was simulated with the calculated impedances. A transmission line length of 9,2 cm was selected. The propagation speed was not adjusted because the influence was negligible.

```
-- Parameters of MTL
constant Zdiff    : Real := 2*53.8144;     -- Z_diff =2*Z_odd
constant Zcom  : Real := 104.422/2.0;   -- Z_com =0.5*Z_even
Lossless : ENTITY MTL_common_differential_lossless(lossless)
        generic map (Zdiff  => Zdiff,    -- differential mode line impedance
                     Zcom   => Zcom,     -- common mode line impedance
                     vdiff  => 172.9e6,  -- diff propagation speed
                     vcom   => 172.9e6,  -- common propagation speed
                     length => 0.092)    -- line length [m]
```

Simulation and measurement results are compared in Figure 86. Resonances of transmission and reflection S-parameters are simulated with good accuracy. Deviations of less than 10 % between the amplitudes are obtained.

The simulation results can be improved if the gap S in the physical parameters is decreased to 0,45 mm. The impedances in the transmission line model are modified to $Z_{odd} = 52.5059$ and $Z_{even} = 105.219$. In Figure 87 the measured and simulated curves are very similar with maximum deviation of about 3 %. For further investigations the original parameter set will be chosen. The influence of the differences between the parameter sets on simulation results is very low.

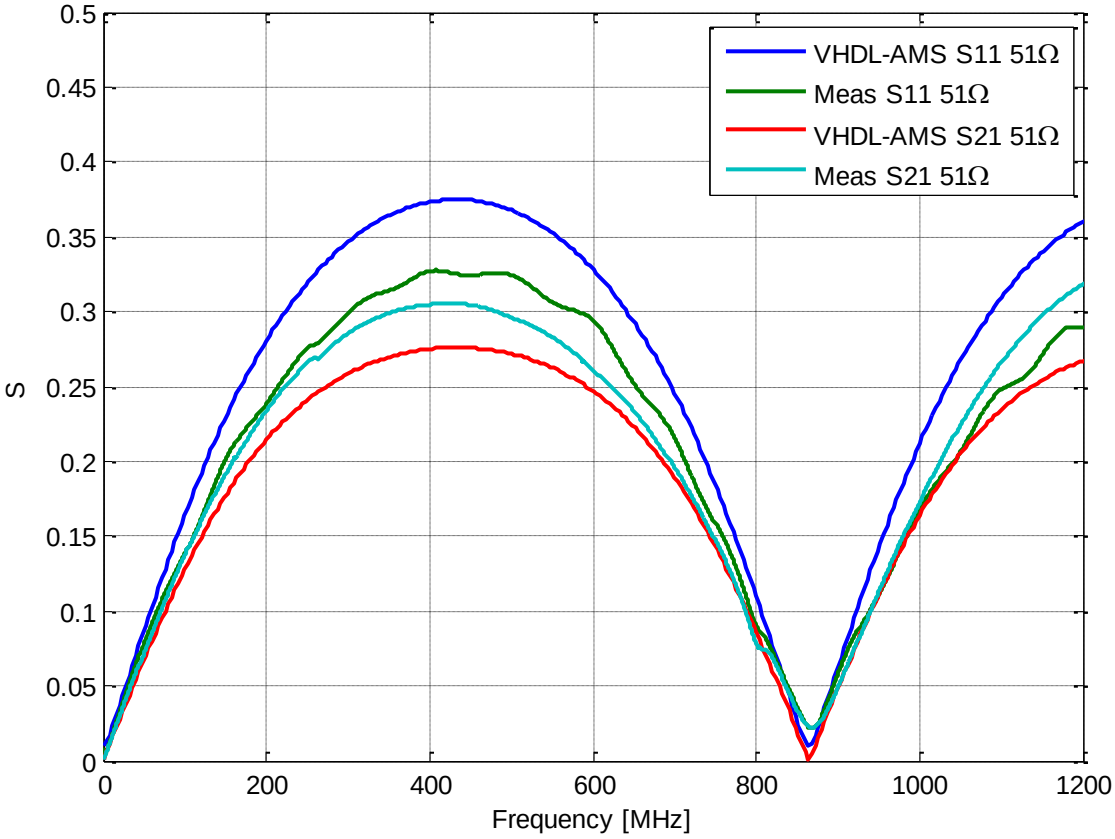

Figure 86: Simulation and measurement results with gap = 0,5 mm

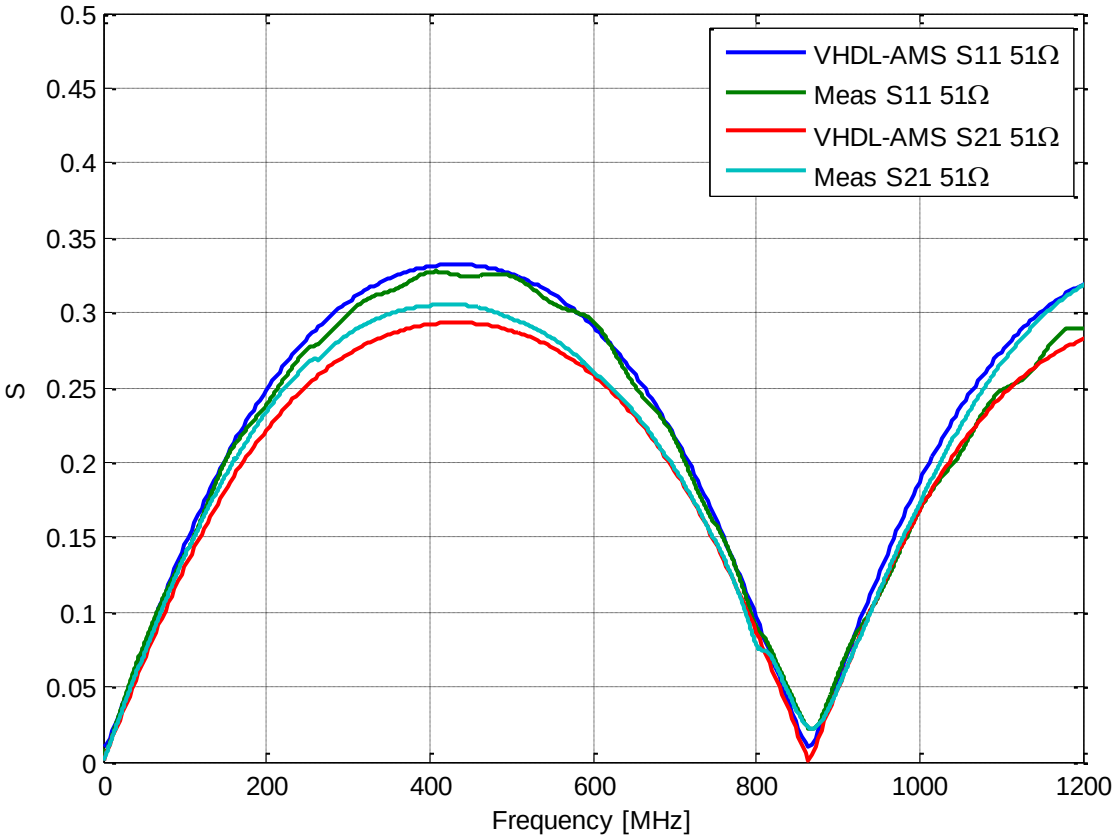

Figure 87: Simulation and measurement results with gap = 0,45 mm

4.2 Measurement of cross-talk signals in time domain

In this section the simulation model of the coupled PCB trace set is verified in time domain. Two pulse generators are discharged into the PCB traces. Two configurations with low and high load resistances of the coupled traces on the cross-talk section on the demonstrator PCB are considered to cover capacitive and inductive coupling effects.

4.2.1 IEC ESD Generator

Figure 88 shows the measurement setup for the IEC generator. The current through both conductors is measured via Tektronix CT1 sensors and voltages are measured at 50 Ω instrument impedance of the oscilloscope. Both traces are terminated on the side of the discharge point with SMD devices to ground. The IEC generator is discharged via a soldering pad close to the SMD device of one transmission line. The charging voltage is set to 1 kV.

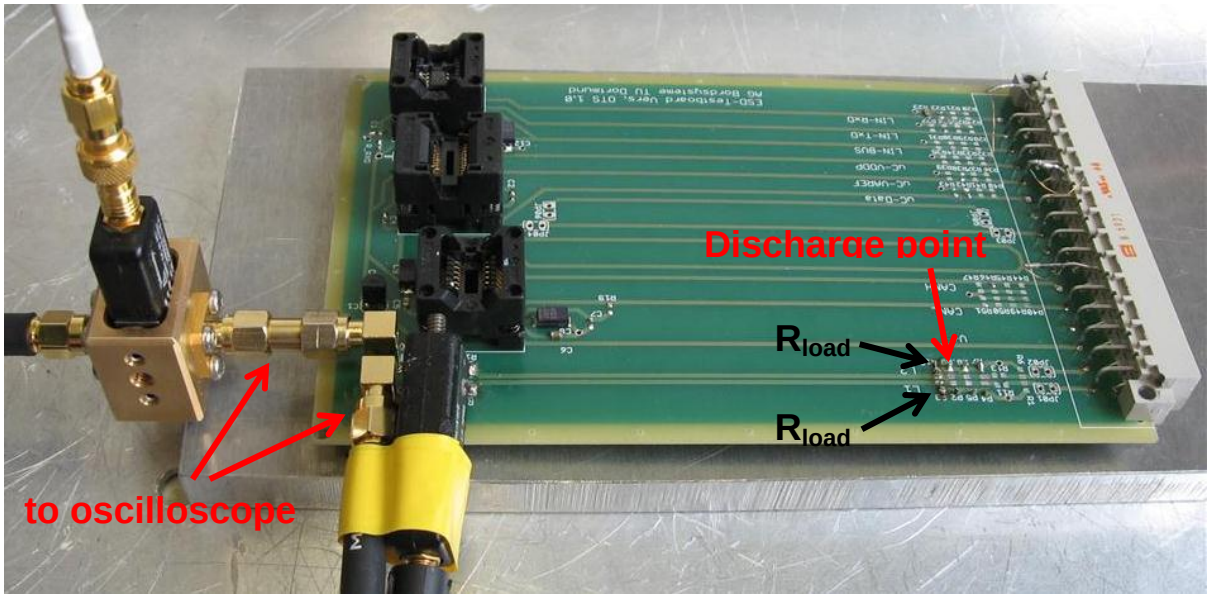

Figure 88: Measurement setup with CT1 current sensors for IEC generator discharge

4.2.1.1 Measurement and simulation results for R_{load} = 1 kΩ

The measurement and simulation results are presented for R_{load} = 1 kΩ at nodes N1 and N3 defined in the sketch in Figure 89.

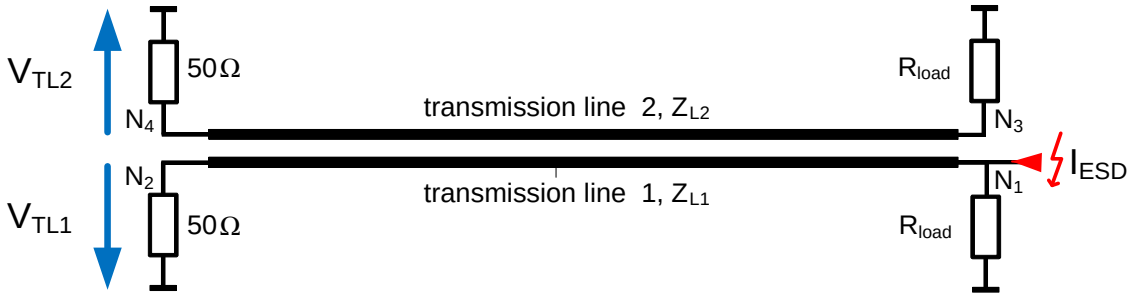

Figure 89: Measurement setup for cross-talk test with IEC generator on demonstrator PCB

Results for voltage and current at node N2 are shown in Figure 90 and Figure 91. The simulated coupled signals at node N4 are compared to the measured shapes in Figure 92 and Figure 93.

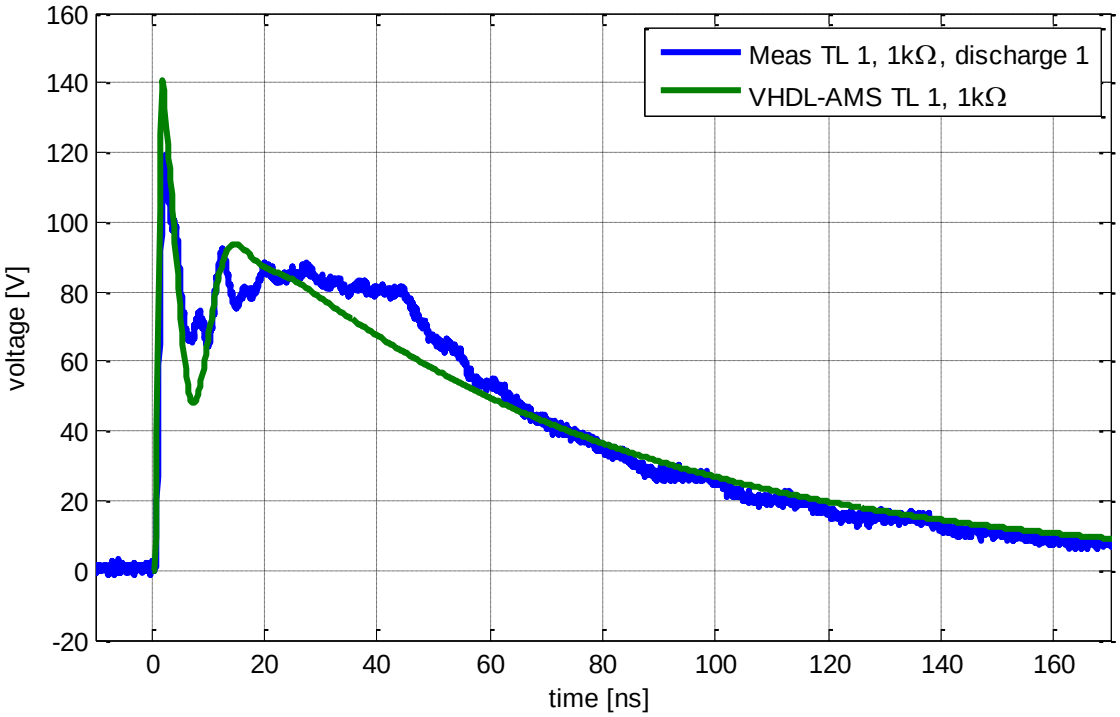

Figure 90: Measured and simulated voltage for 1 kV IEC generator discharge on TL1

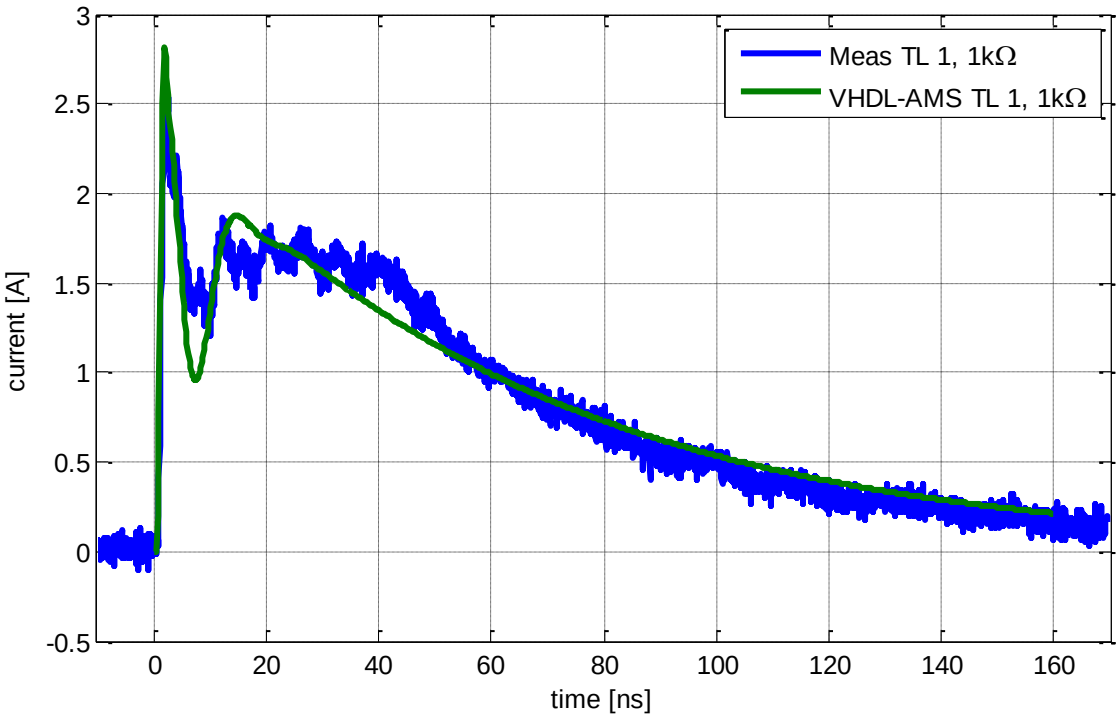

Figure 91: Measured and simulated current for 1 kV IEC generator discharge on TL1

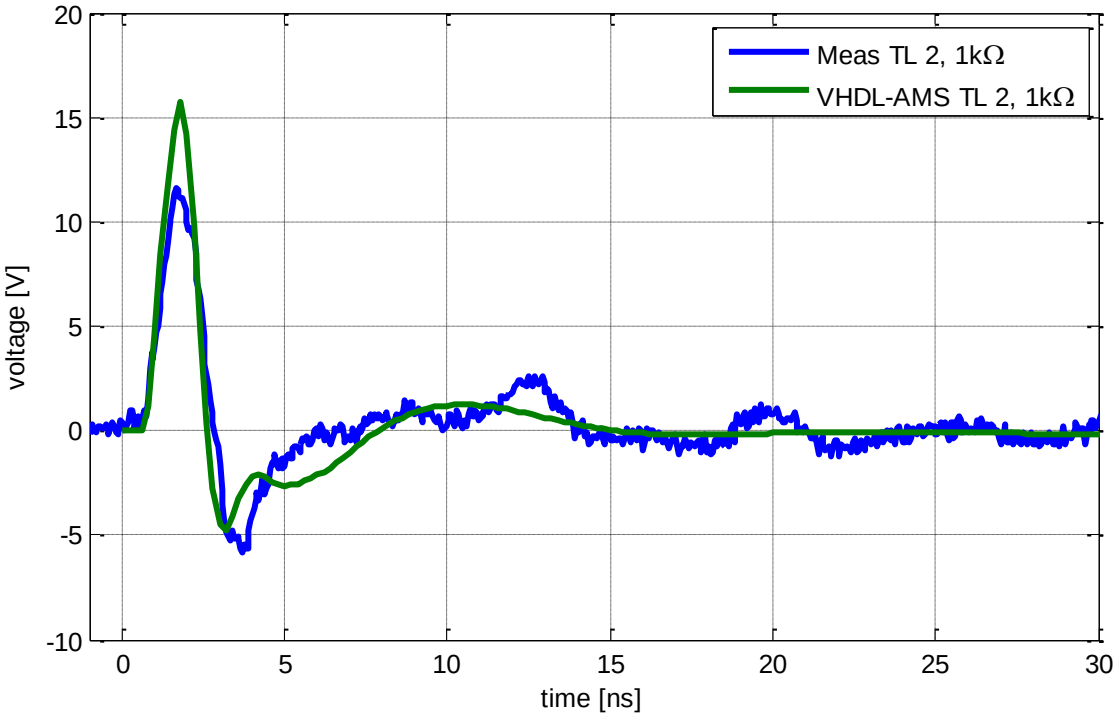

Figure 92: Measured and simulated voltage for 1 kV IEC generator discharge on TL2

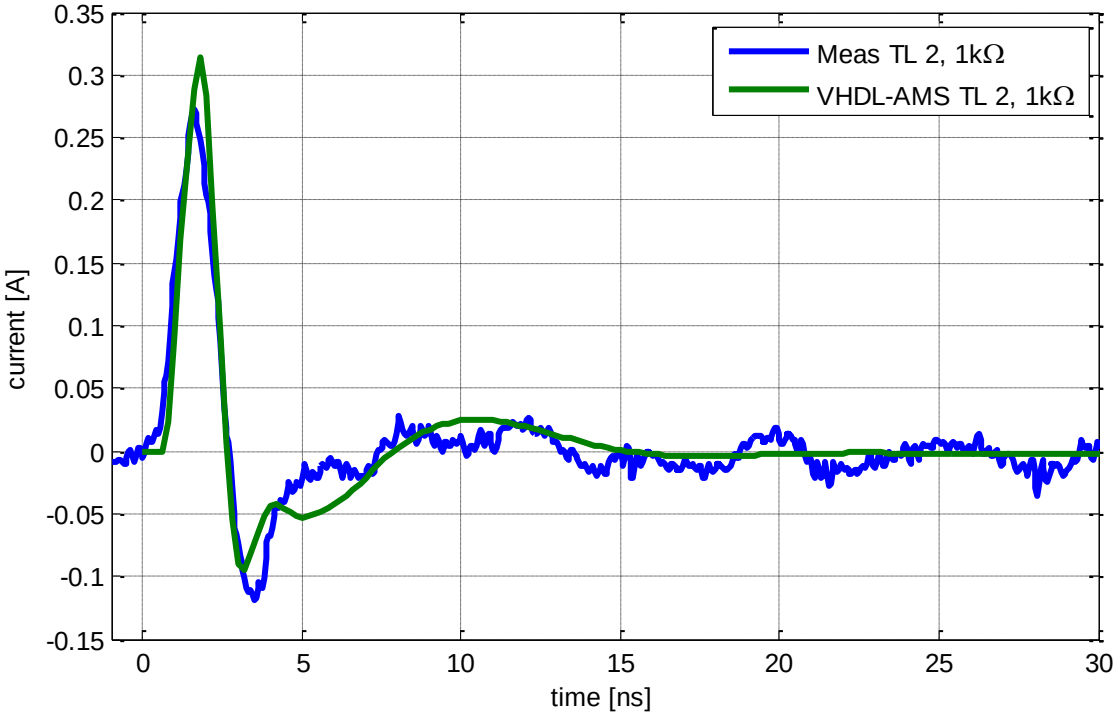

Figure 93: Measured and simulated current for 1 kV IEC generator discharge on TL2

All presented curves show a good matching between measurement and simulation. According to Table 18 only 2,5 % deviation is obtained if the calculated energies are compared for trace 1. A higher deviation between measurement and simulation was calculated for trace 2 due to noise problems. Absolute deviations are very small. Concerning the coupling factor only about 5 nJ or about 2000 times less energy was measured on trace 2.

TL	measurement	simulation	deviation
1	8,0 µJ	8,2 µJ	2,5 %
2	3,9 nJ	4,9 nJ	25 %

Table 18: Comparison of measured and simulated energies for IEC ESD generator

	Energy N2 - trace 1	Energy N4 - trace 2	Coupling factor (E_{N2}/ E_{N4})
Simulation	8.2 µJ	4.9 nJ	1740
Measurement	8.0 µJ	3.9 nJ	2051

Table 19: Coupling factors for measured and simulated data

4.2.1.2 Measurement and simulation results for R_{load} = 0,47 Ω

All transmission lines are terminated with 0,47 Ω SMD devices except from node N1 where the IEC generator is discharged. The coupling current signal on conductor 2 is measured via a CT1 current sensor as shown in Figure 94.

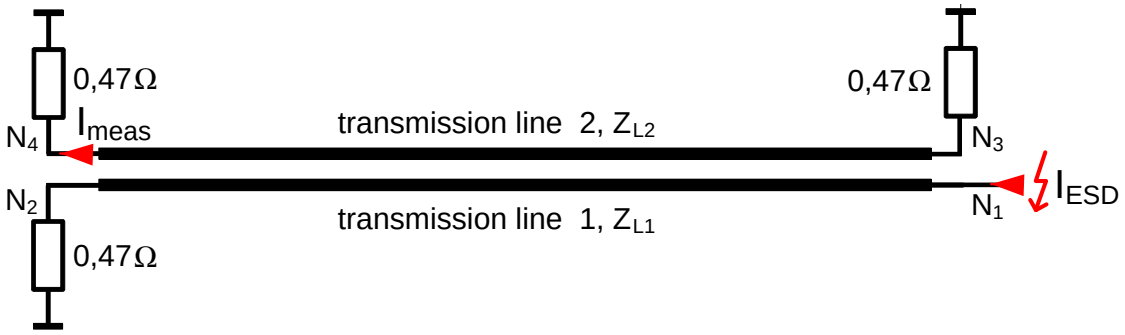

Figure 94: Measurement setup for cross-talk test with IEC generator and R_{load} = 0,47 Ω

In comparison to the case R_{load} = 1 kΩ the peak current in Figure 95 rises up to about 1,5 A. The simulated and measured current shapes show a good matching.

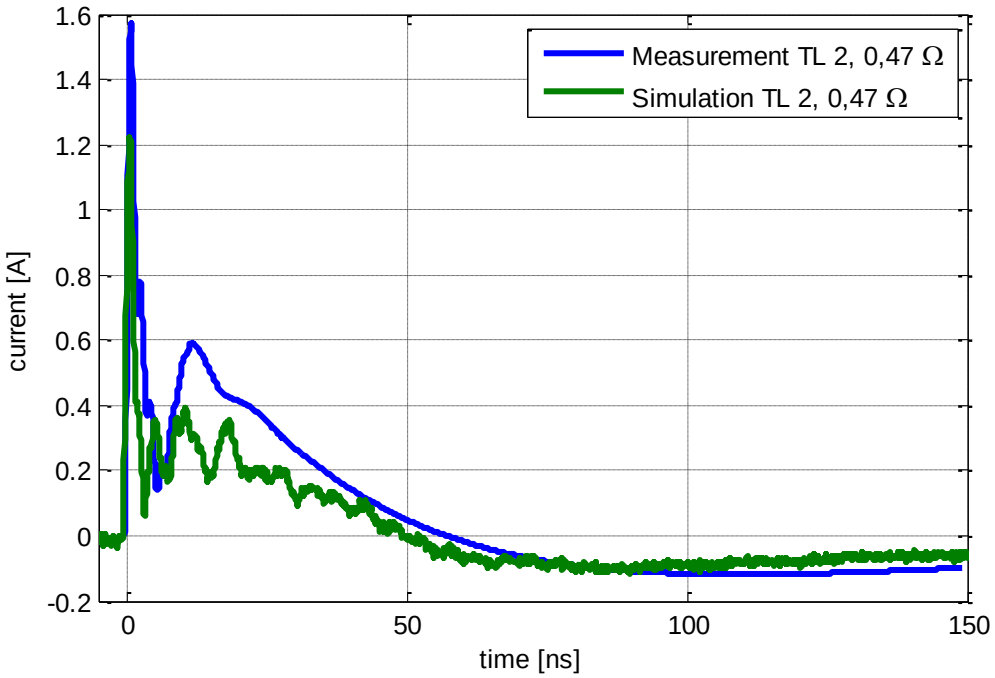

Figure 95: Measured and simulated current through transmission line 2 for 0,47 Ω termination

4.2.2 **TLP**

Similar to the investigation with the IEC generator in this section results are shown that were created with a TLP. The charging voltage of the TLP was set to 400 V. Figure 96 and Figure 97 show a schematic of the setup. The TLP is discharged via trace 1 so that the trace is terminated by 50 Ω impedance of the TLP and by R_{load}.

Only the discharge current can be measured. On transmission line 2 voltage and current shapes were measured.

Figure 96: Measurement setup for cross-talk test with TLP on demonstrator PCB

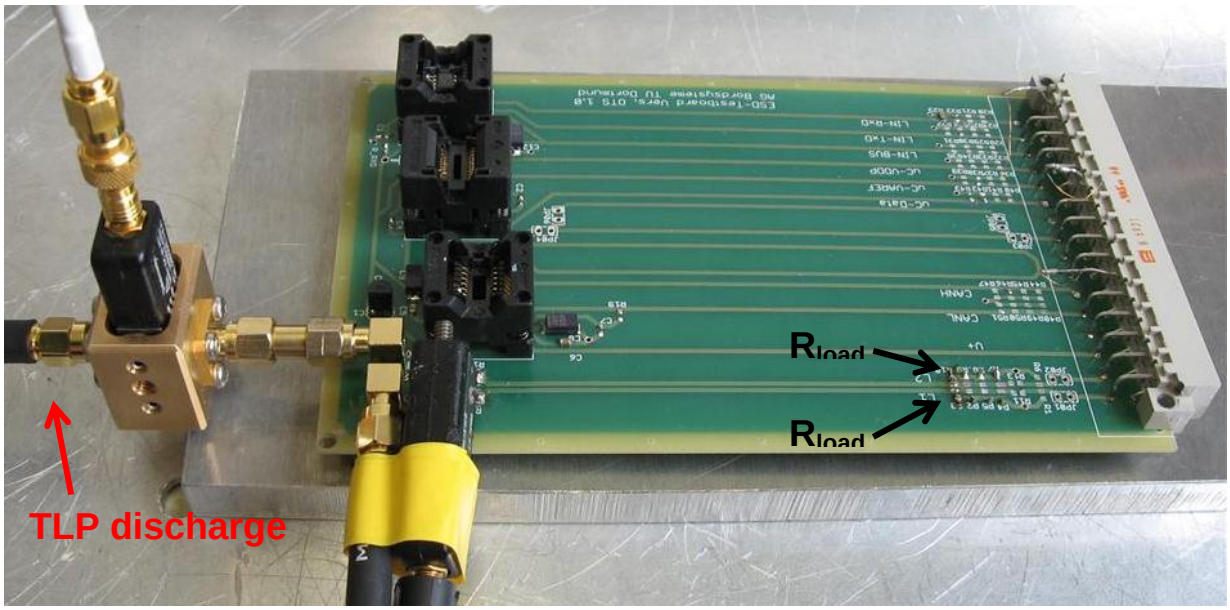

Figure 97: Measurement setup with CT1 current sensors for TLP discharge

4.2.2.1 Measurement and simulation results for R_{load} = 51 Ω

In Figure 98 to Figure 100 measurement and simulation results are shown for R_{load} = 51 Ω. All measured curves can be reproduces well with simulation. Current amplitude of about 4 A is reached with 50 Ω termination and series instrument impedance. On transmission line 2 the maximum amplitude is about 400 mA. The coupling factor of the current is about 10.

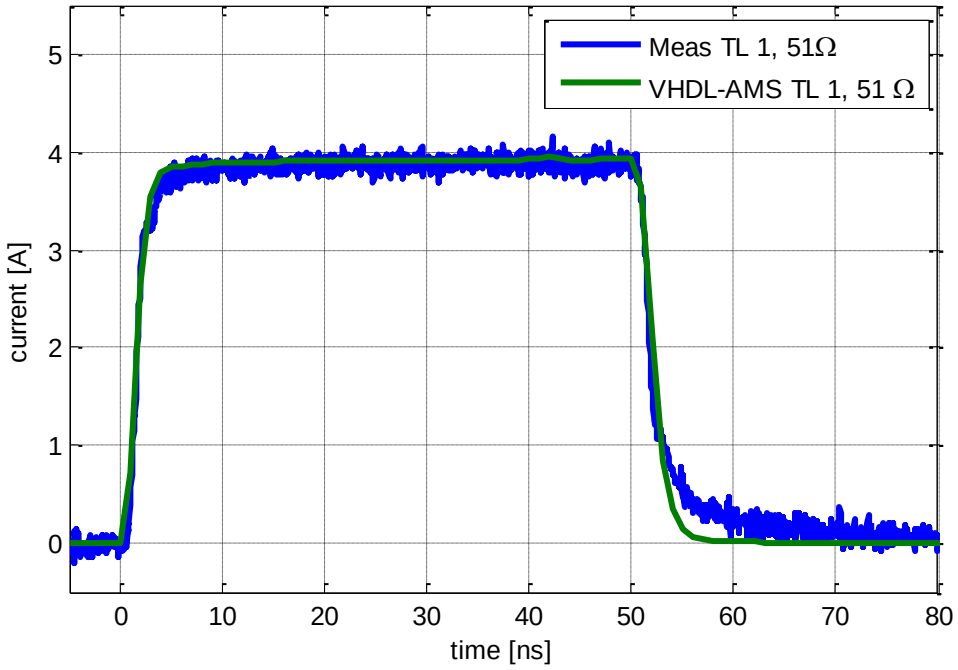

Figure 98: Measured and simulated current for 400 V TLP discharge on TL1

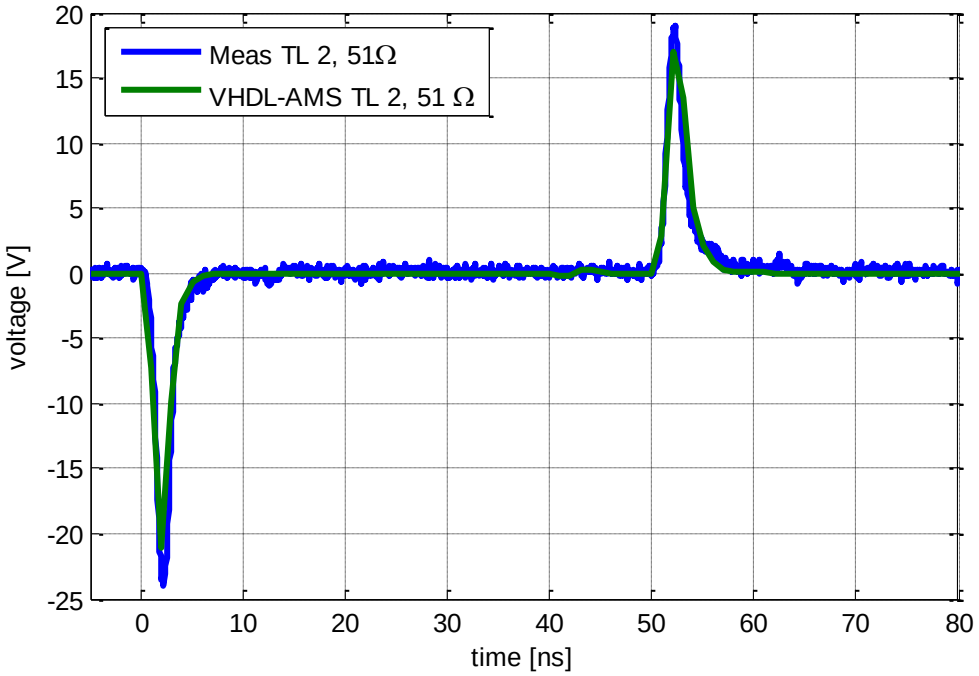

Figure 99: Measured and simulated voltage for 400 V TLP discharge on TL2

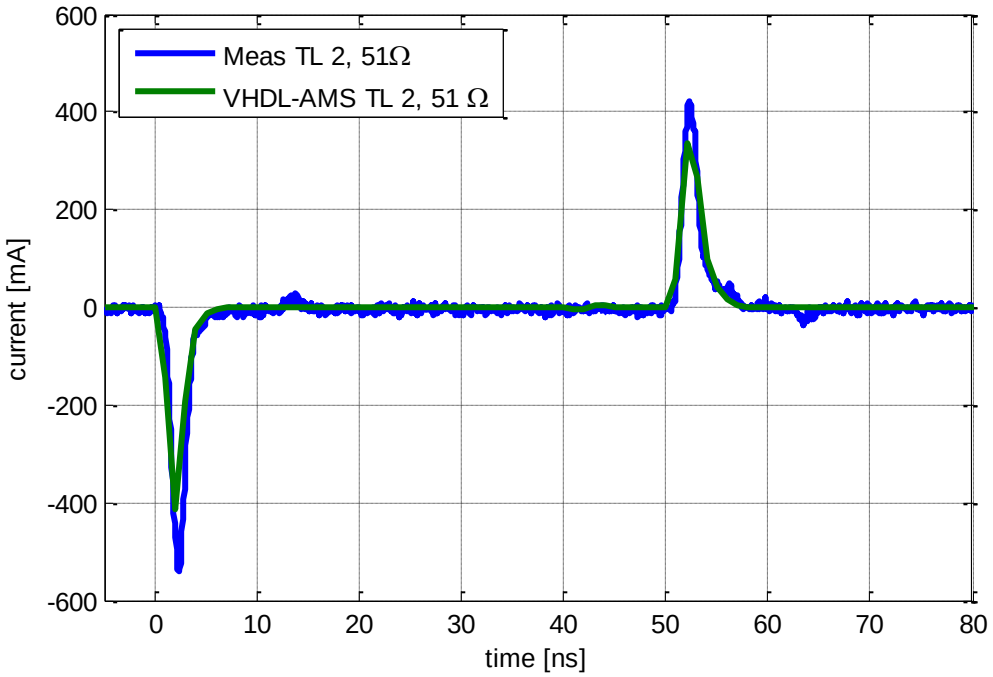

Figure 100: Measured and simulated current for 400 V TLP discharge on TL2

The deviation between simulated and measured energies on transmission line 2 is about 14 %, i.e. below the measurement error.

TL	measurement	simulation	deviation
2	25,7 nJ	22,2 nJ	-14 %

Table 20: Comparison of measured and simulated energies for TLP

4.2.2.2 Measurement and simulation results for R_{load} = 0,47 Ω

In this section results are presented for 0,47 Ω terminations. Current amplitudes of about 8 A are obtained on trace 1 for 400 V charging voltage because of low resistance. In Figure 102 and Figure 103 the measured and simulated currents are compared. Significant deviations of the current amplitudes on trace 2 were simulated. This might be caused by additional inductances in the measurement setup. The simulation is very sensitive for small variations of R_{load}. In Figure 104 R_{load} was replaced by 1 Ω and 10 nH inductance.

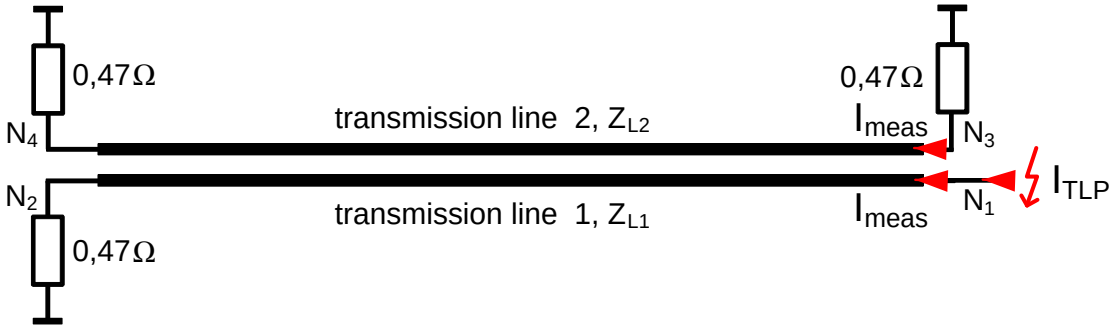

Figure 101: Measurement setup for cross-talk test with TLP and R_{load} = 0,47 Ω

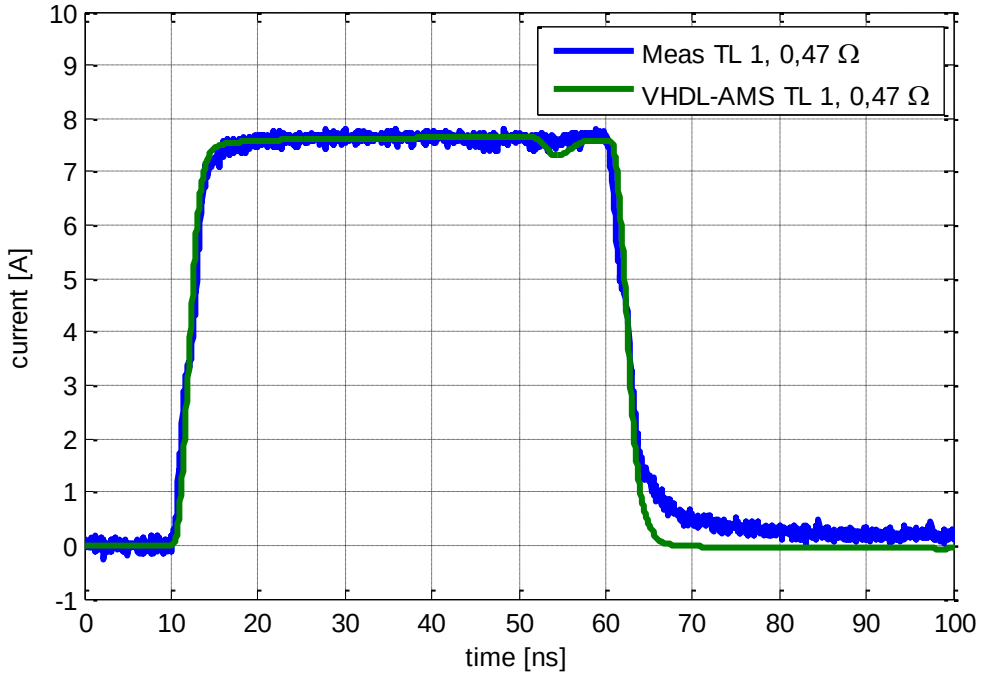

Figure 102: Comparison of simulated and measured current on TL1

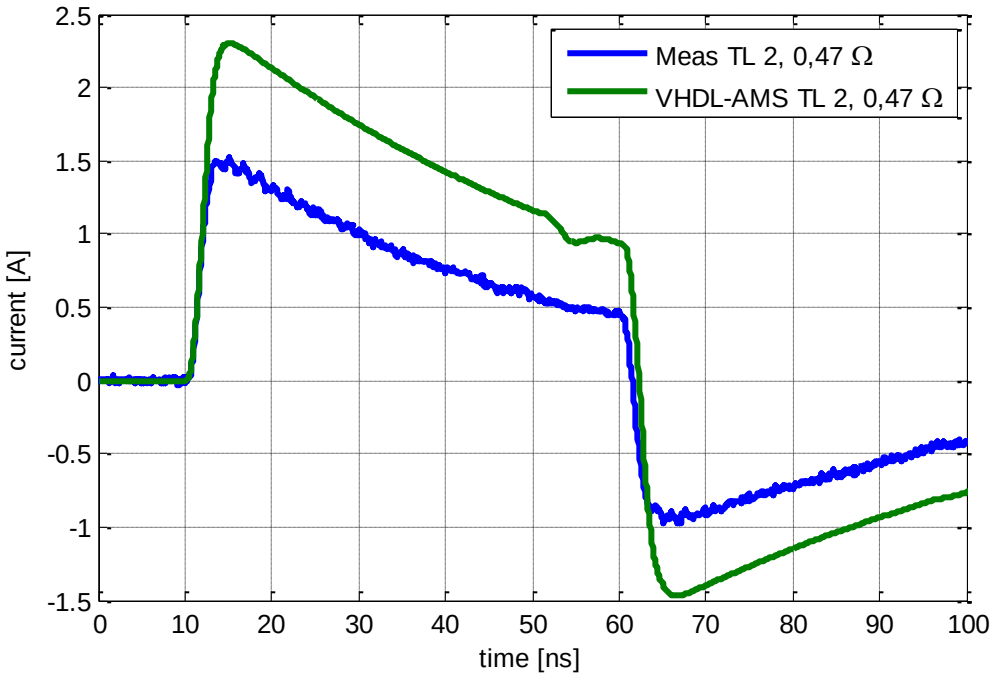

Figure 103: Comparison of simulated and measured current on TL2

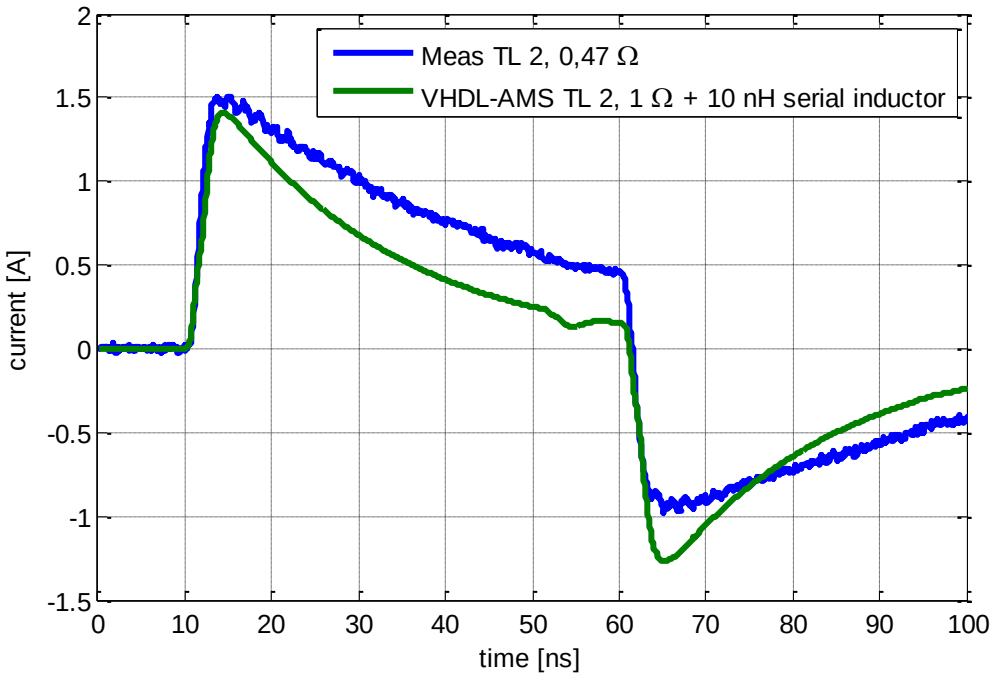

Figure 104: Simulated current with additional resistance and inductance

4.3 Impact of protection elements on currents

In this section simulation of coupling signals with selected models of ESD protection elements is compared to measurement.

4.3.1 **Setup**

Current and voltage shapes on both transmission lines were measured in the cross-talk section of the demonstrator PCB. In the setup shown in Figure 105 the protection element (PE) is connected parallel to an 1 kΩ resistor at transmission line 2. The IEC ESD generator is discharged at node N1 via conductor 1. For observation, if the breakdown voltage of the protection devices is exceeded, voltage and current are measured with an oscilloscope at trace 2 at node N4 for 1 kV and 8 kV charging voltage.

Figure 105: Setup for measurement of coupling signals with ESD protection elements

4.3.2 **Measurement results**

A 10 nF capacitor, Protek TVS GBLCS05C diode and the EPCOS CT0603K14G varistor were selected as ESD protection elements for investigation.

4.3.2.1 10 nF capacitor

In Figure 106 and Figure 107 the measured and simulated curves for 1 kV charging voltage are compared. The voltage amplitude exceeds 20 V. If the charging voltage of the IEC generator is set to 8 kV nearly 200 V and 4 A peaks can be measured. All curves show a good matching.

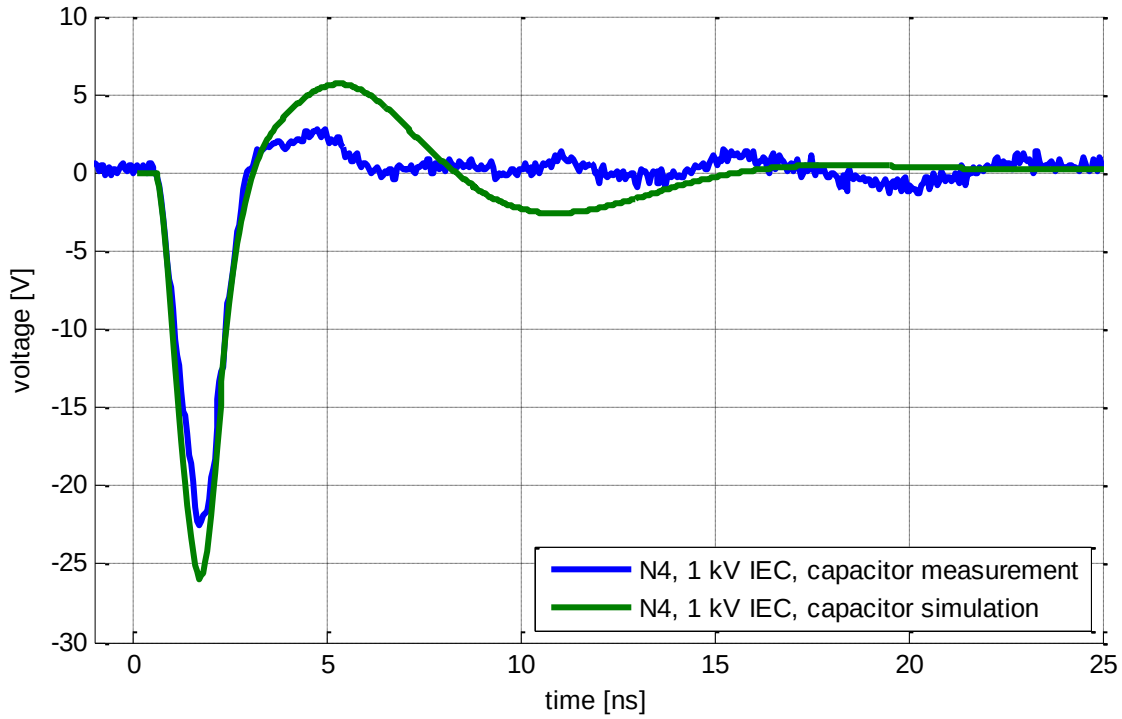

Figure 106: Voltage at node N4 with 10 nF capacitor on TL2 for 1 kV discharge on TL1

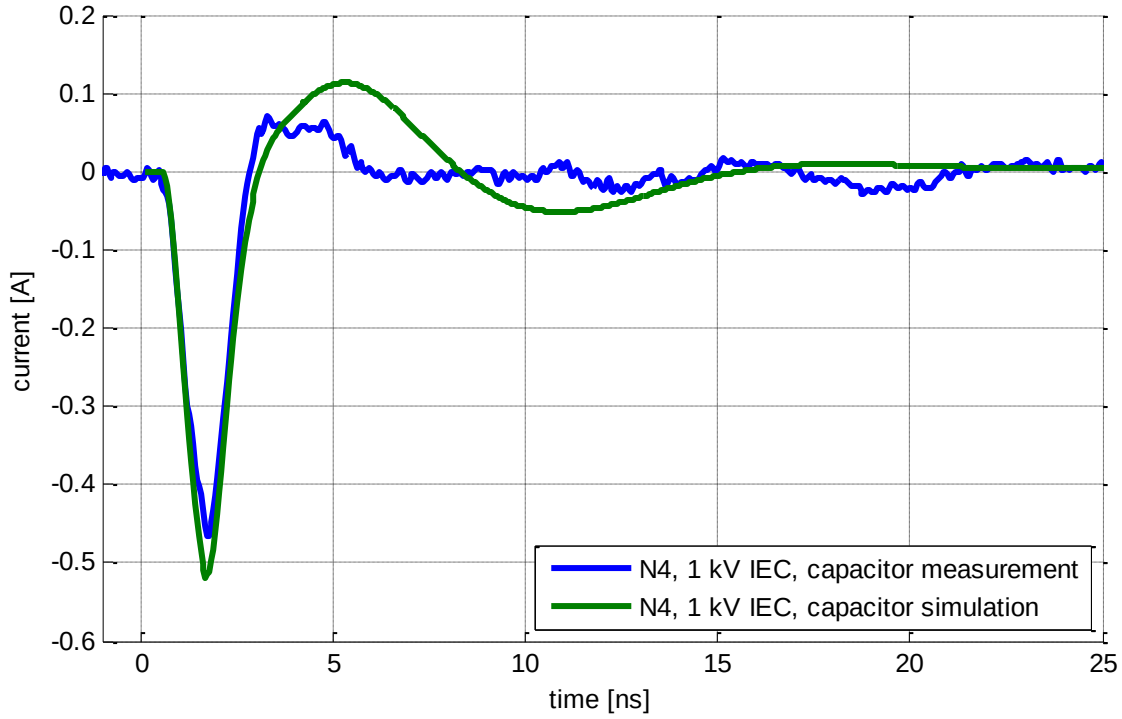

Figure 107: Current through node N4 with 10 nF capacitor on TL2 for 1 kV discharge on TL1

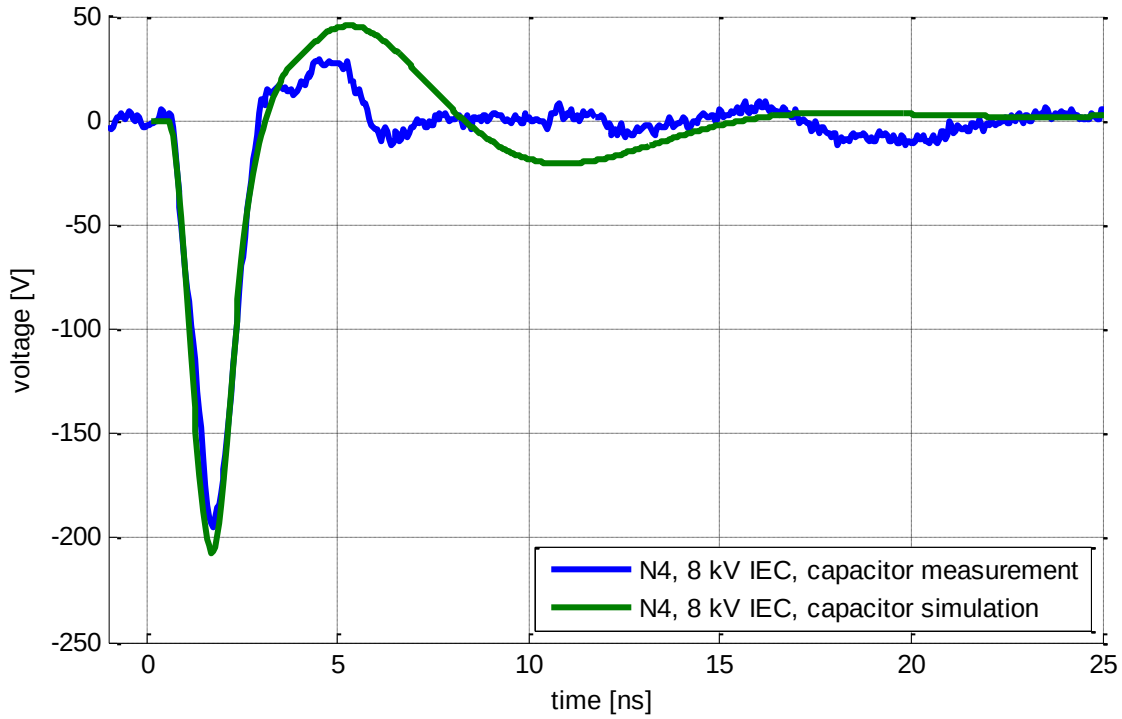

Figure 108: Voltage at node N4 with 10 nF capacitor on TL2 for 8 kV discharge on TL1

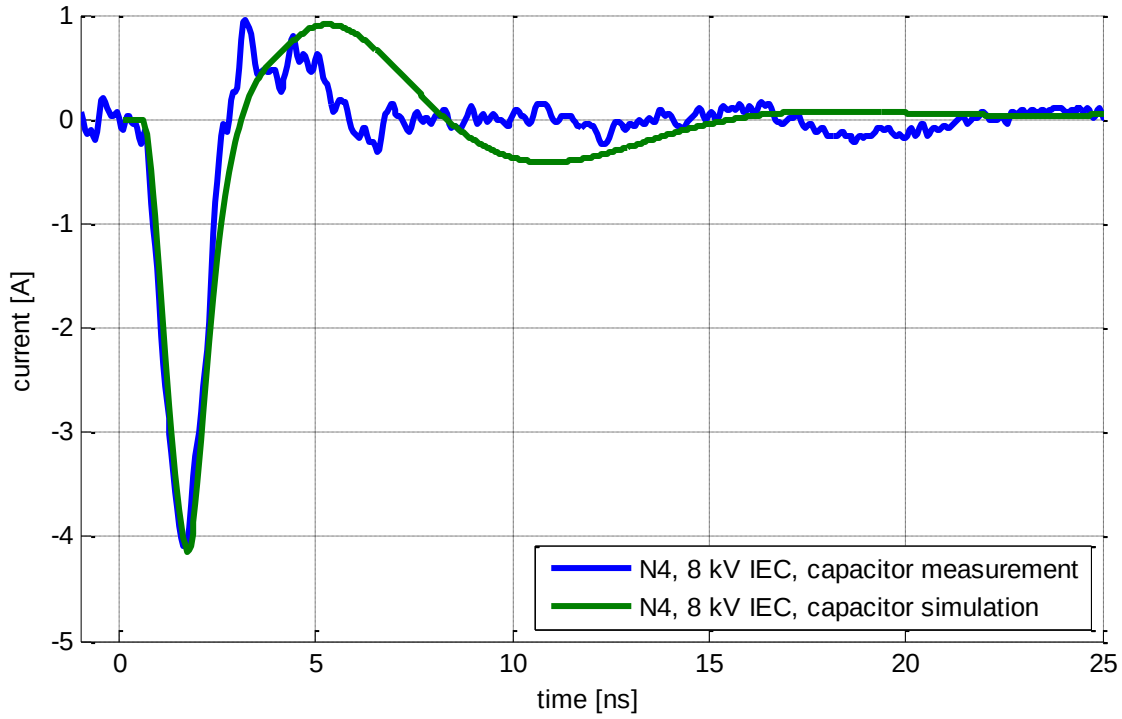

Figure 109: Current through node N4 with 10 nF capacitor on TL2 for 8 kV discharge on TL1

4.3.2.2 Diode Protek TVS GBLCS05C

Similar pulse shapes are obtained if a TVS diode is connected parallel to trace 2. Data for 1 kV and 8 kV charging voltage are compared in Figure 110 to Figure 113. Because of the IV characteristic and lower capacitance of the device the peak amplitudes are lower compared to the 10 nF capacitor. The rise time of the peak amplitudes is similar to the first peak of the IEC generator.

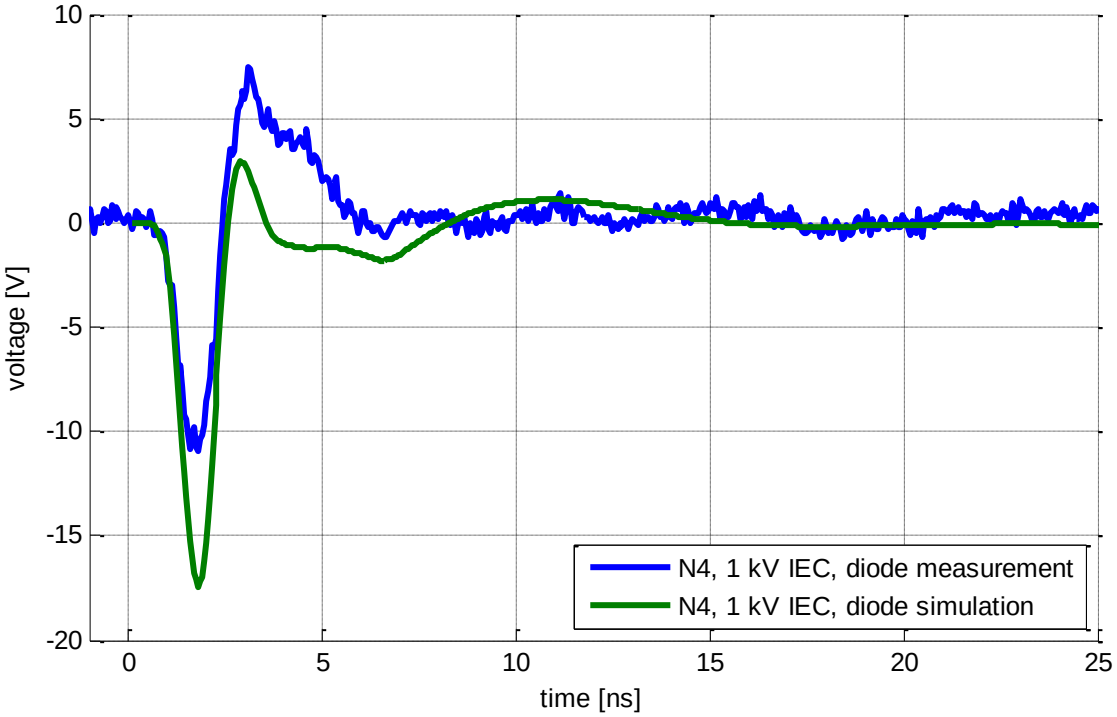

Figure 110: Voltage at node N4 with Protek TVS diode on TL2 for 1 kV discharge on TL1

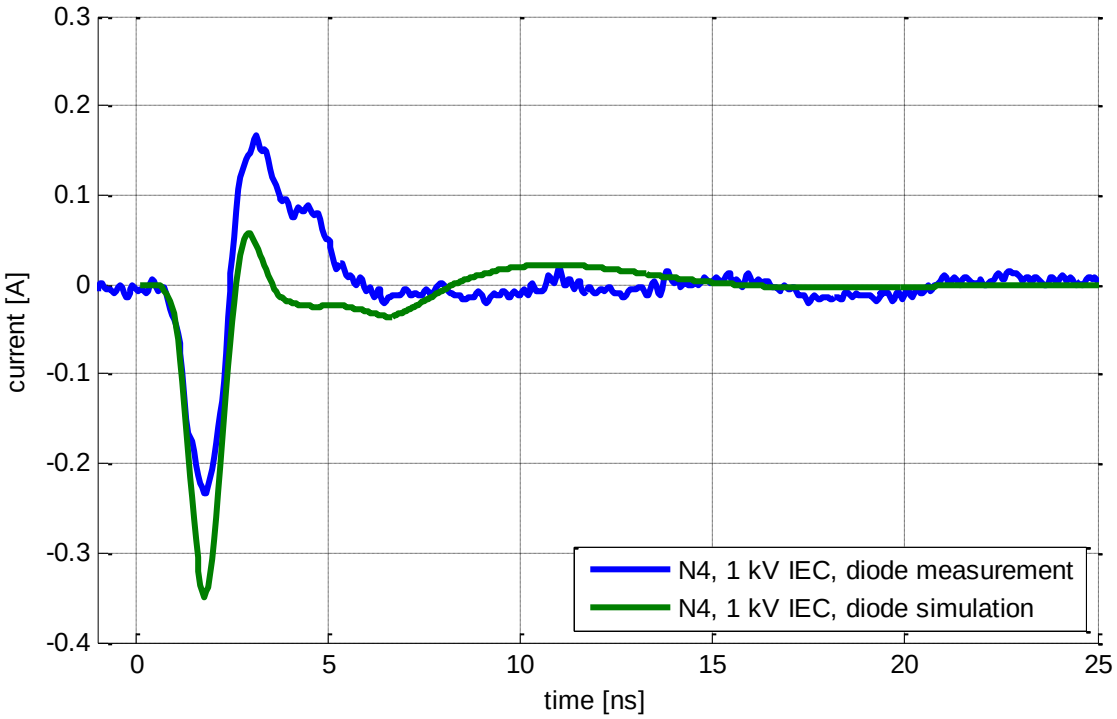

Figure 111: Current through node N4 with Protek TVS diode on TL2 for 1 kV discharge on TL1

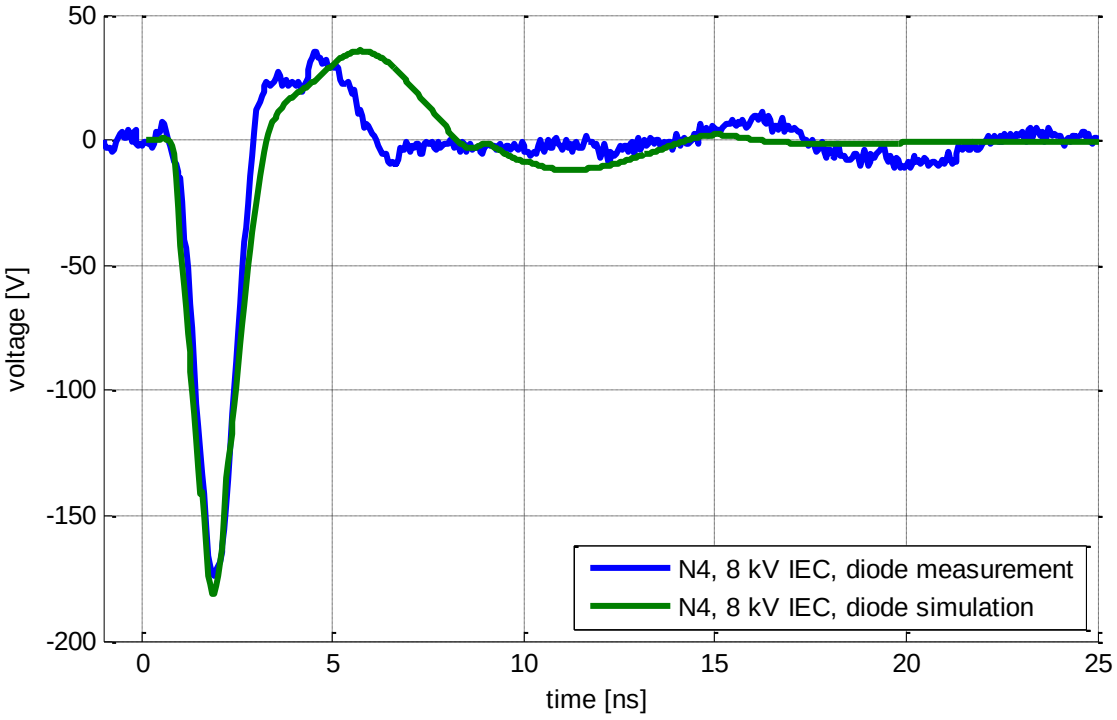

Figure 112: Voltage at node N4 with Protek TVS diode on TL2 for 8 kV discharge on TL1

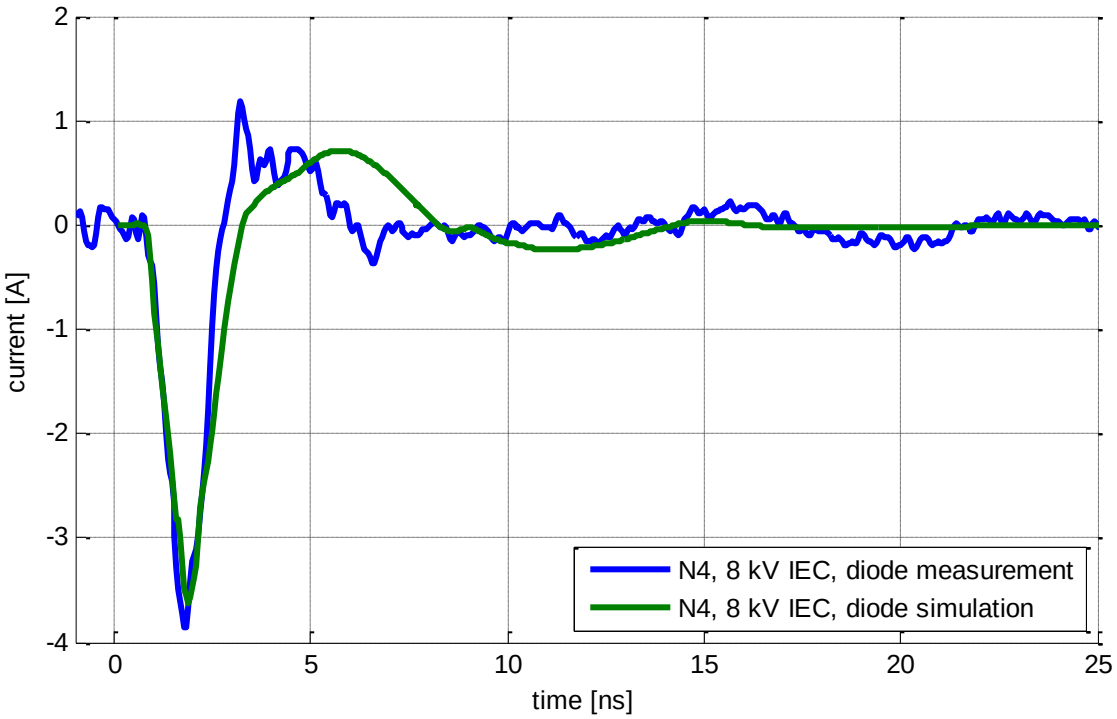

Figure 113: Current at node N4 with Protek TVS diode on TL2 for 8 kV discharge on TL1

4.3.2.3 Varistor EPCOS CT0603K14G

Good simulation results are obtained for the varistor. The peak amplitudes in Figure 114 to Figure 117 match well with measured data. Similar pulse shapes were observed with the diode.

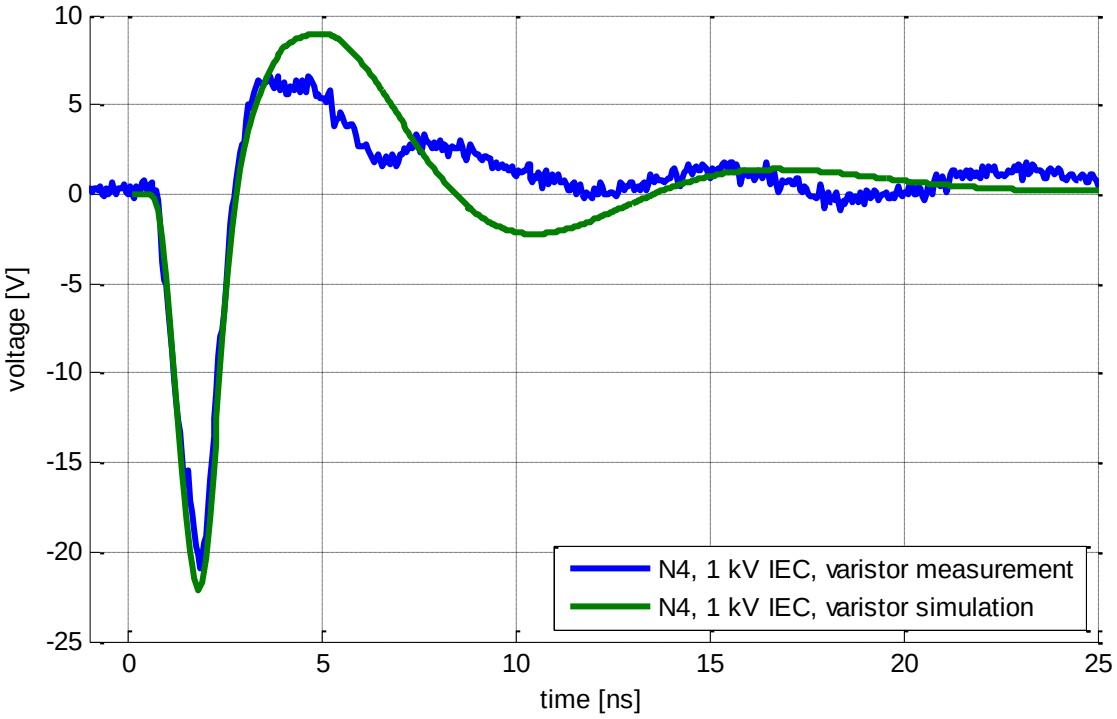

Figure 114: Voltage at node N4 with EPCOS varistor on TL2 for 1 kV discharge on TL1

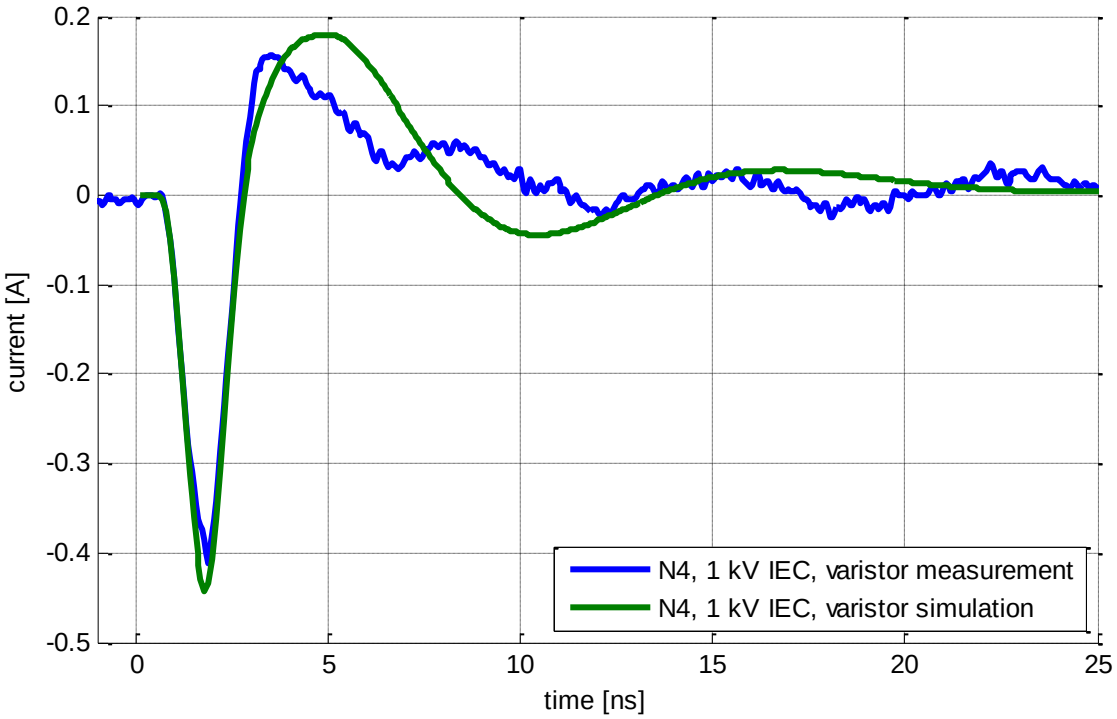

Figure 115: Current through node N4 with EPCOS varistor on TL2 for 1 kV discharge on TL1

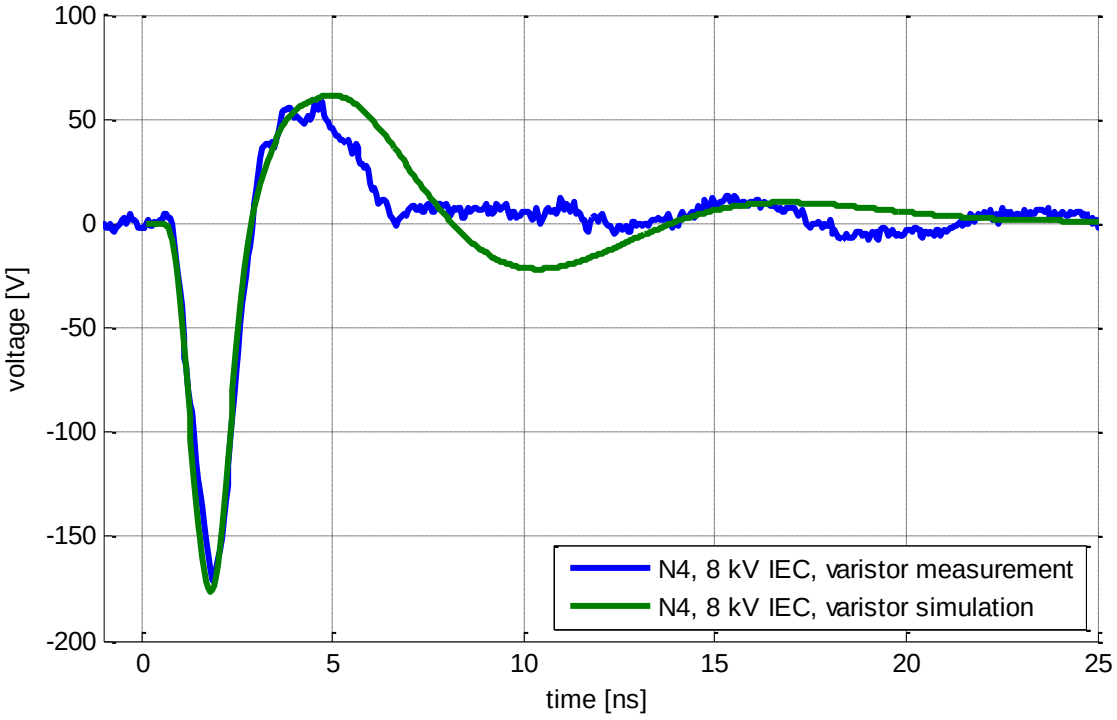

Figure 116: Voltage at node N4 with EPCOS varistor on TL2 for 8 kV discharge on TL1

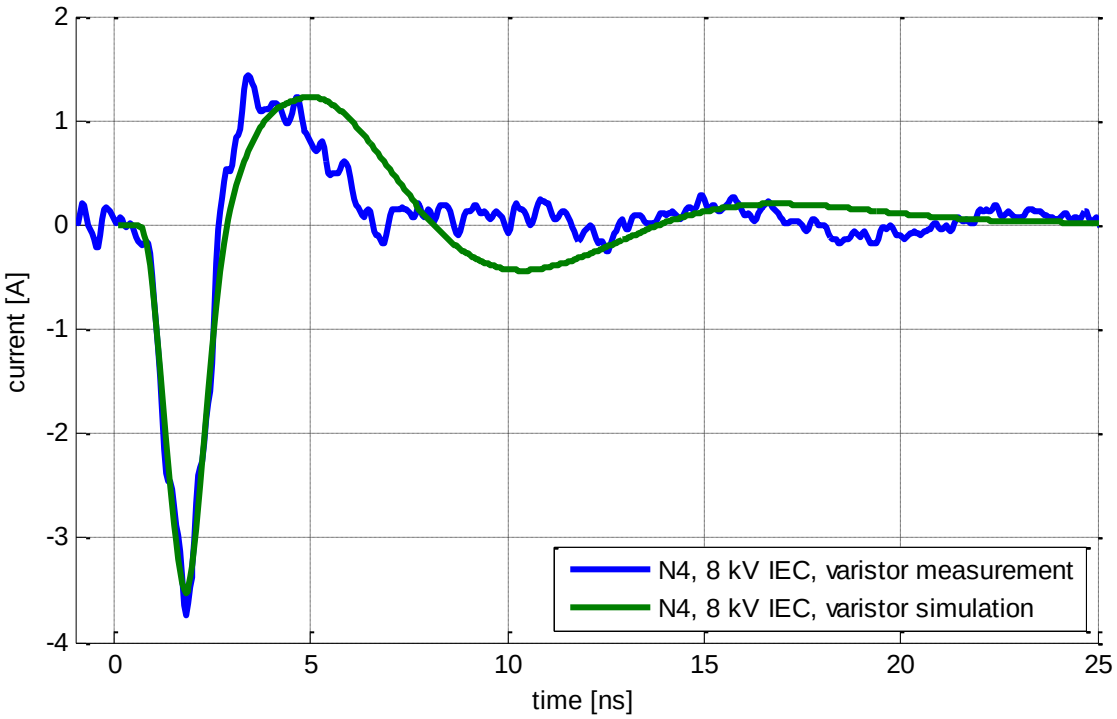

Figure 117: Current through node N4 with EPCOS varistor on TL2 for 8 kV discharge on TL1

4.4 Measurement of IEC robustness on demonstrator PCB

Different IC pins were characterized using the TLP setup. IC models were implemented in the electrical and thermal domain from the characterization data. In this section the simulated failure behavior is compared to measurement using the IEC ESD generator and the demonstrator PCB. Three discharges within 3 s were performed per voltage level. To avoid pre-damaging effects a new IC was used for each voltage level. Three ICs were tested with increasing voltages until a significant rise in the current consumption could be measured. The minimum step of charging voltage was 0,5 kV.

4.4.1 **Setup**

For testing the ESD robustness of IC pins on system level the ESD generator is discharged via the connector pin of the demonstrator PCB. Figure 118 gives an overview of the setup. The discharge current through a short additional wire soldered in the PCB current path was measured with a CT1 or CT6 current sensor and an oscilloscope. The setup is shown in Figure 119. During discharge the IV source meter was not connected. For additional investigations ESD protection elements were connected parallel to PCB pads close to the connector pin. The ESD pulse propagates through a 10 cm transmission line to the IC pin. In this case the conductor was modeled as a single transmission line. The impedance can be calculated using a microstrip configuration e.g. in the program TXLINE. For the adjusted parameters shown in Figure 120 the line impedance in the simulation model was set to 83 Ω.

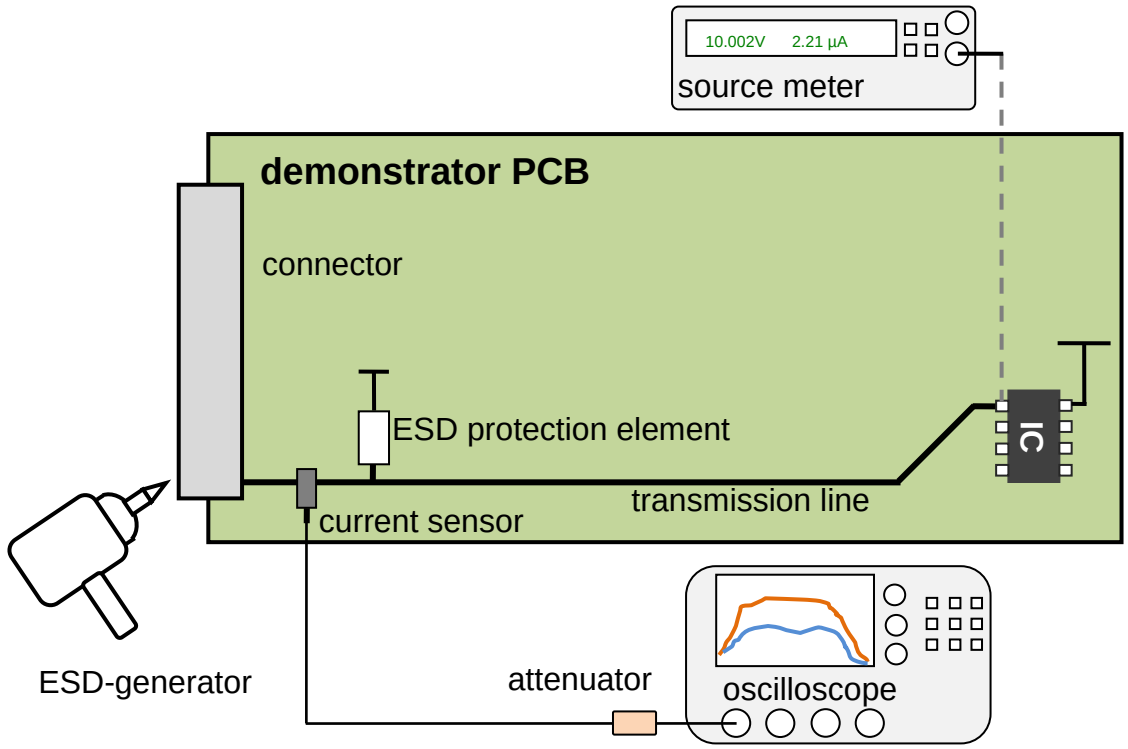

Figure 118: Measurement setup with IC

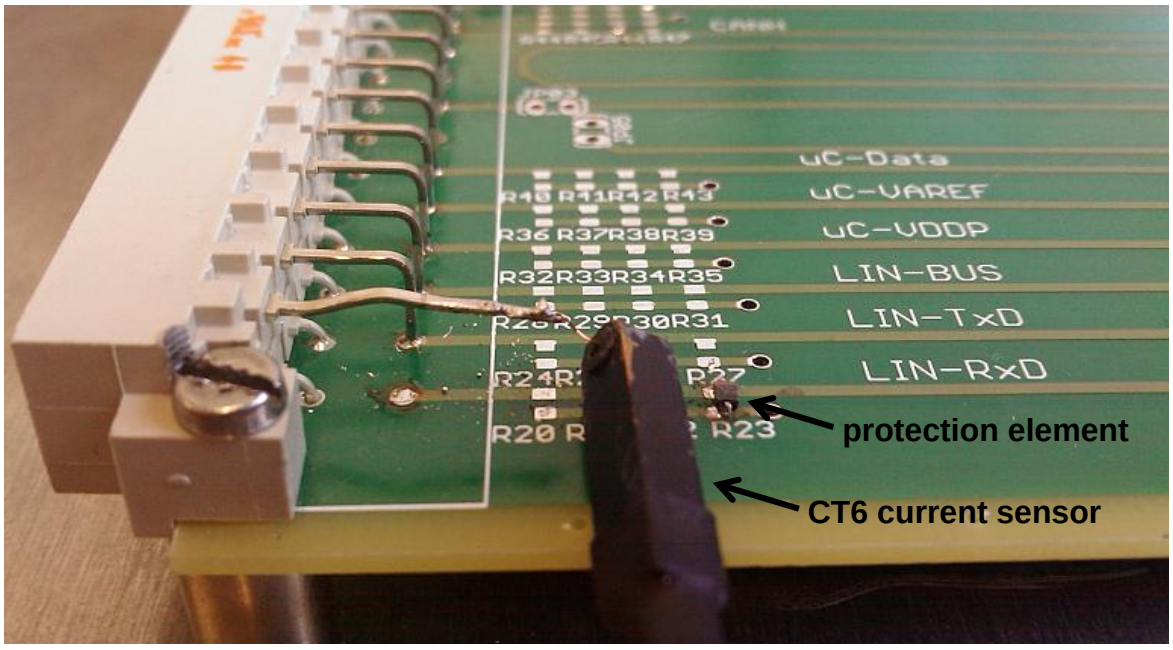

Figure 119: Demonstrator PCB with CT6 current sensor

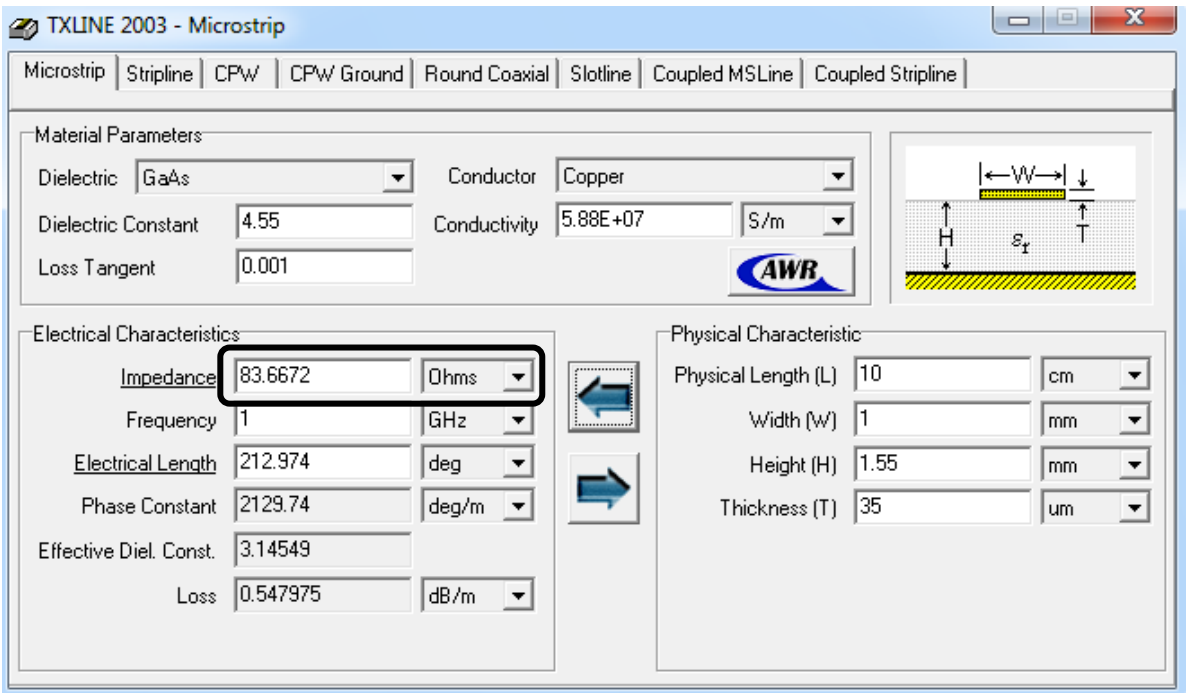

Figure 120: Calculation of stripline impedance with TXLINE

The equivalent simulated circuit is shown in Figure 121. The effect of the connector on the current shape was modeled by a 2 nH inductor and a parallel 1 pF capacitor. Similar to the TLP setup the IC socket inductance was included in the ground path of the IC. I_{sim} is the simulated discharge current through the connector. I_{IC} and V_{IC} are simulated current and voltage shapes at the IC pin which will be compared to measured amplitudes obtained with the TLP setup.

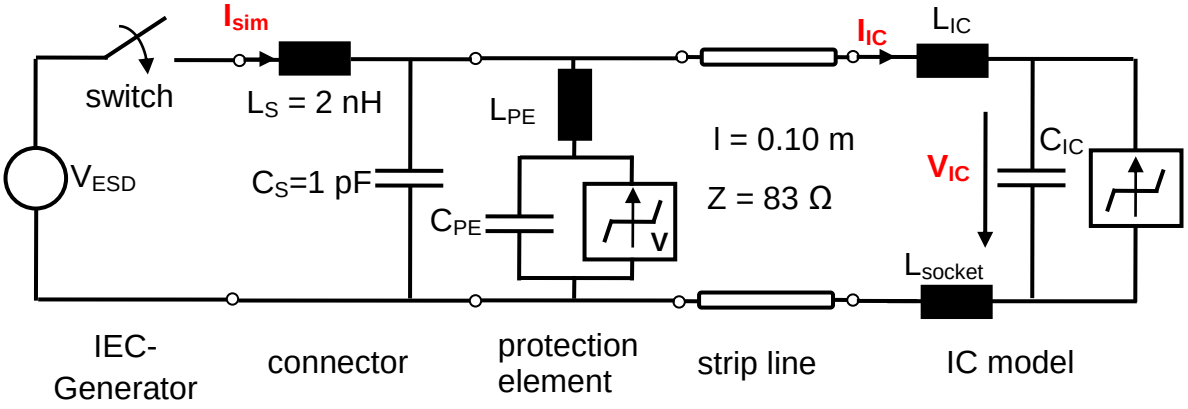

Figure 121: Equivalent simulation setup

4.4.2 **LIN TxD**

The simulated and measured discharge currents at the connector pin are shown in Figure 122. Permanent damage was detected for a 3 kV IEC generator discharge. The rise time and shape of the first peak of the curves are very similar.

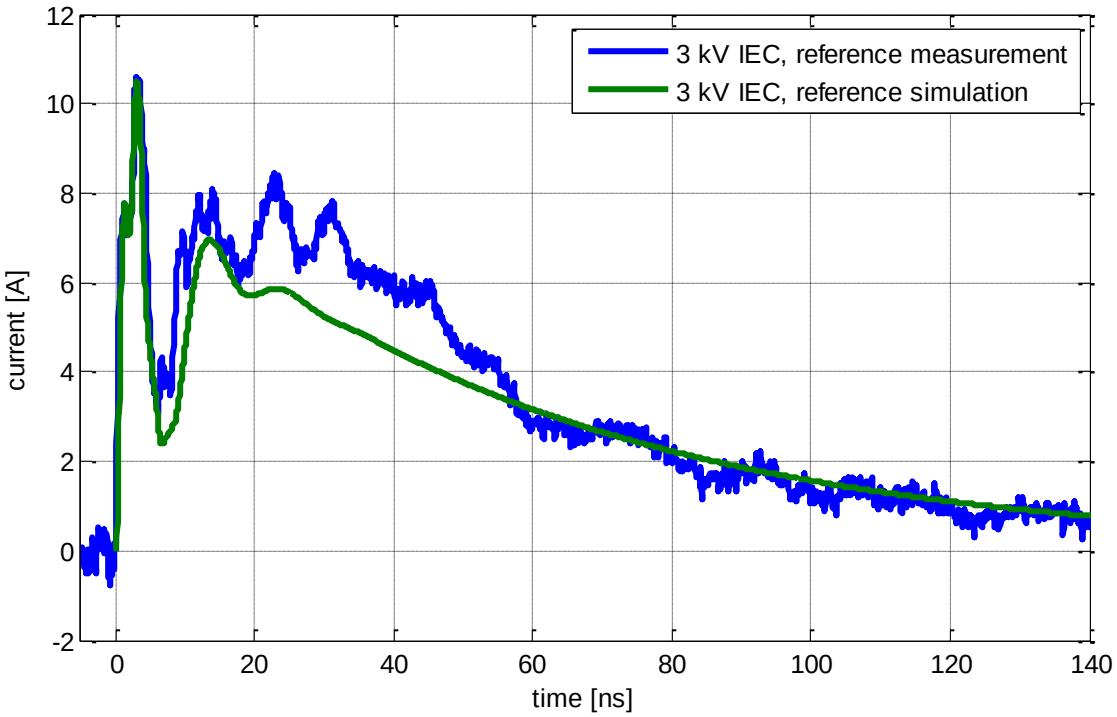

Figure 122: Simulated and measured current for LIN TxD pin at connector of demonstrator PCB

In Figure 123 and Figure 124 the maximum current and voltage amplitudes are compared for TLP and IEC ESD discharges at the detected failure levels. Because measurement of voltage and current at the IC pin on system level with IEC ESD generator is difficult without affecting the test result, the waveforms at the IC pin were simulated and compared to measured results taken with the TLP setup. Maximum TLP amplitudes which cause IC failure are obtained with 25 ns pulse width. In case of the LIN TxD pin the charging voltage was 525 V. The peak voltage of over 50 V was measured compared to 30 V simulated for the IEC generator. This proves that IC failure with IEC ESD discharges is not an overvoltage effect here. The current peak amplitude for 25 ns pulse width is 10 A and about 14 A for the simulated IEC discharge.

The IC models were implemented based on TLP data with 100 ns pulse width. The calculated failure energies of TLP and system level IEC discharges are compared in Table 21. Deviation of about 7 % between the energies is obtained. It is assumed that the IC failure can be referred to the same energy-based mechanism for TLP and IEC discharges.

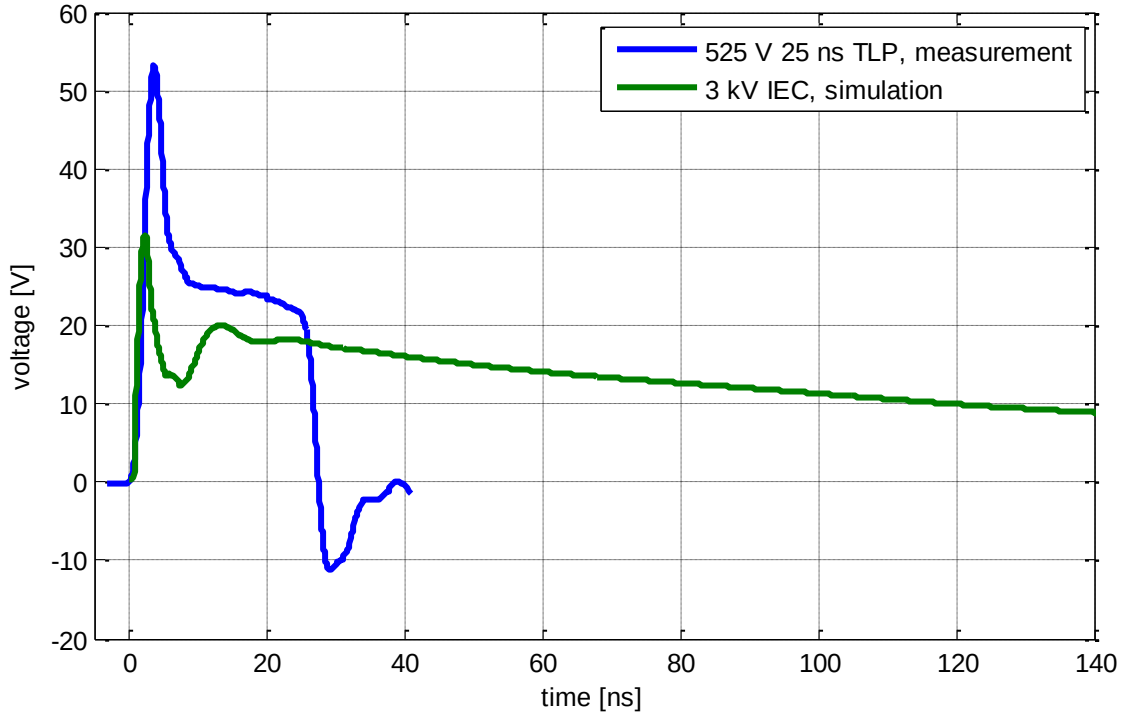

Figure 123: Maximal TLP voltage and IEC generator voltage at LIN TxD pin

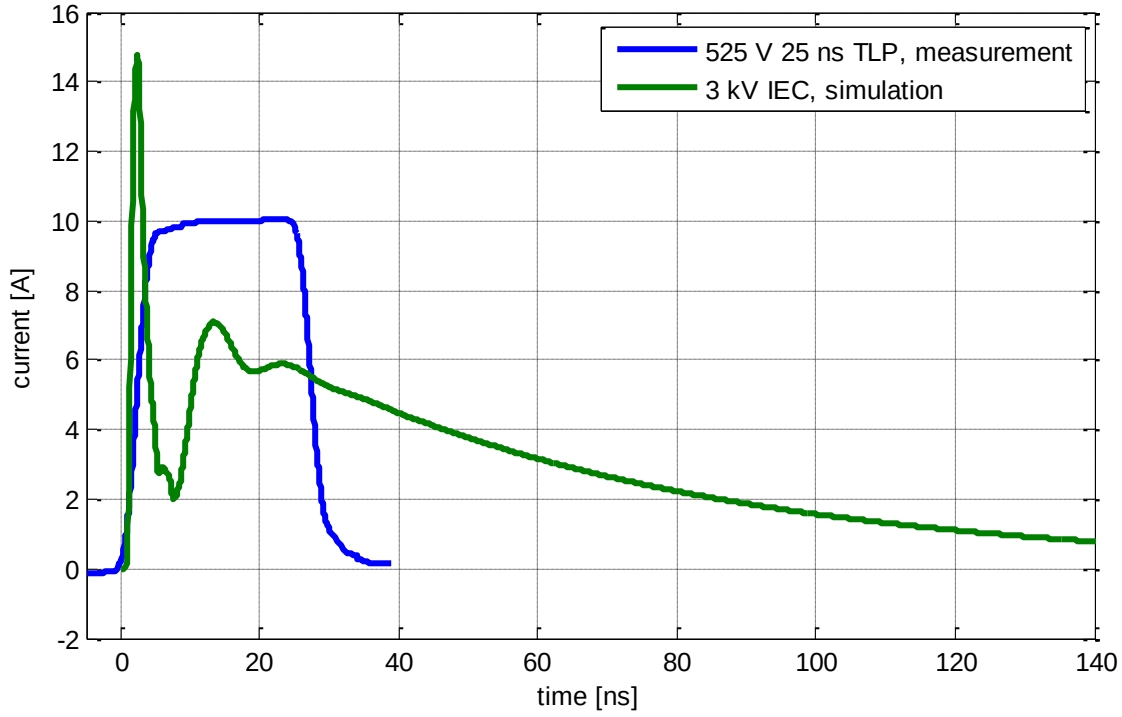

Figure 124: Maximal TLP current and IEC generator current at LIN TxD pin

ESD pulse	V_{ESD} [V]	$V_{IC,max}$ [V]	$I_{IC,max}$ [A]	E_{fail} [µJ]
IEC NoiseKen	3000	31.61	14.74	6.92
TLP 100 ns	250	44.8	4.6	7.4

Table 21: Comparison of IEC and TLP failure energies for LIN TxD pin

4.4.3 **CANH**

The simulated and measured current waveforms for IEC discharges via the CANH pin on the demonstrator PCB are shown in Figure 125. The charging voltage causing IC destruction was 2,5 kV. In the measurement data the high pass characteristics and saturation effects of the CT6 current sensor can be observed after 50 ns.

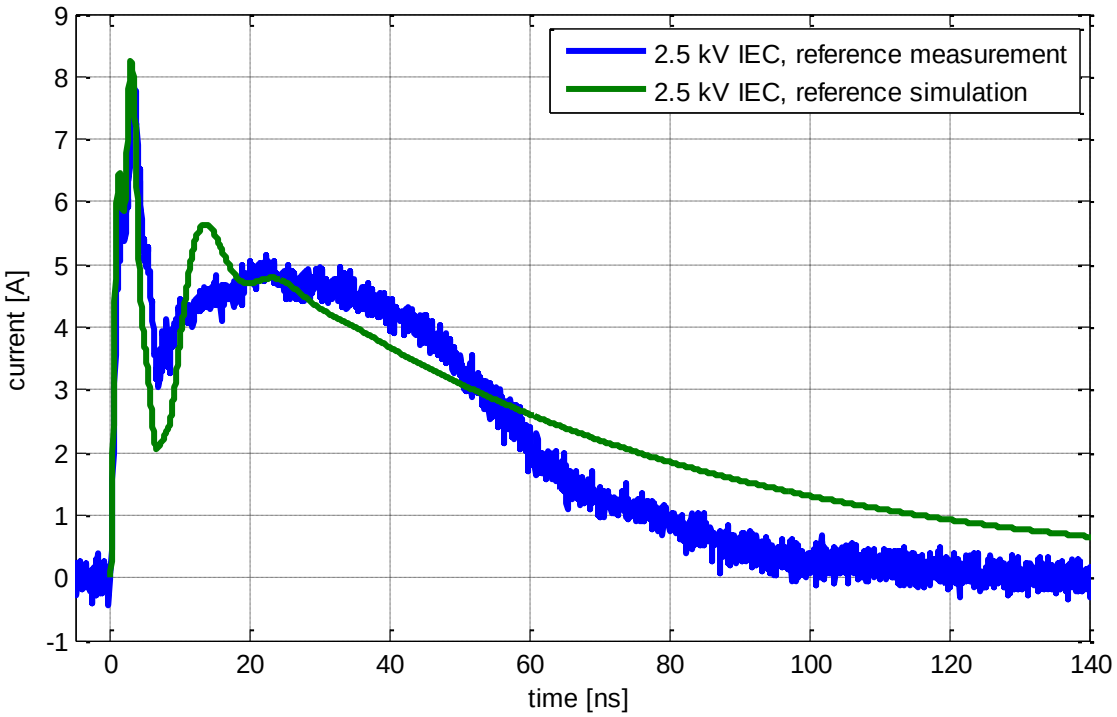

Figure 125: Simulated and measured current for CANH pin at connector of demonstrator PCB

The simulated voltage and current for the IEC discharge are compared to TLP measurement data in Figure 126 and Figure 127. Peak amplitudes of over 120 V and about 7,5 A were measured for 450 V charging voltage and 25 ns pulse width. The voltage peak at the IC pin is about 100 V in case of IEC discharges.

The comparison of the calculated failure energies underlines the assumption that the IC failure due to TLP and IEC discharges is energy-based. The deviation is about 10 %.

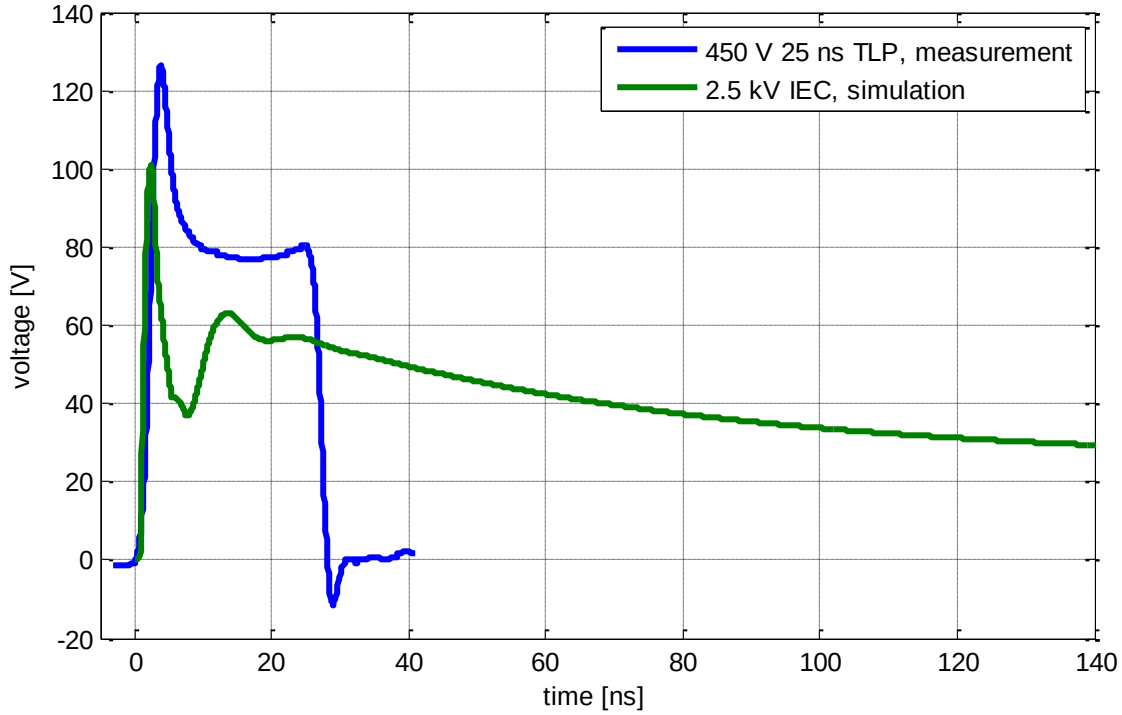

Figure 126: Maximal TLP voltage and IEC generator voltage at CANH pin

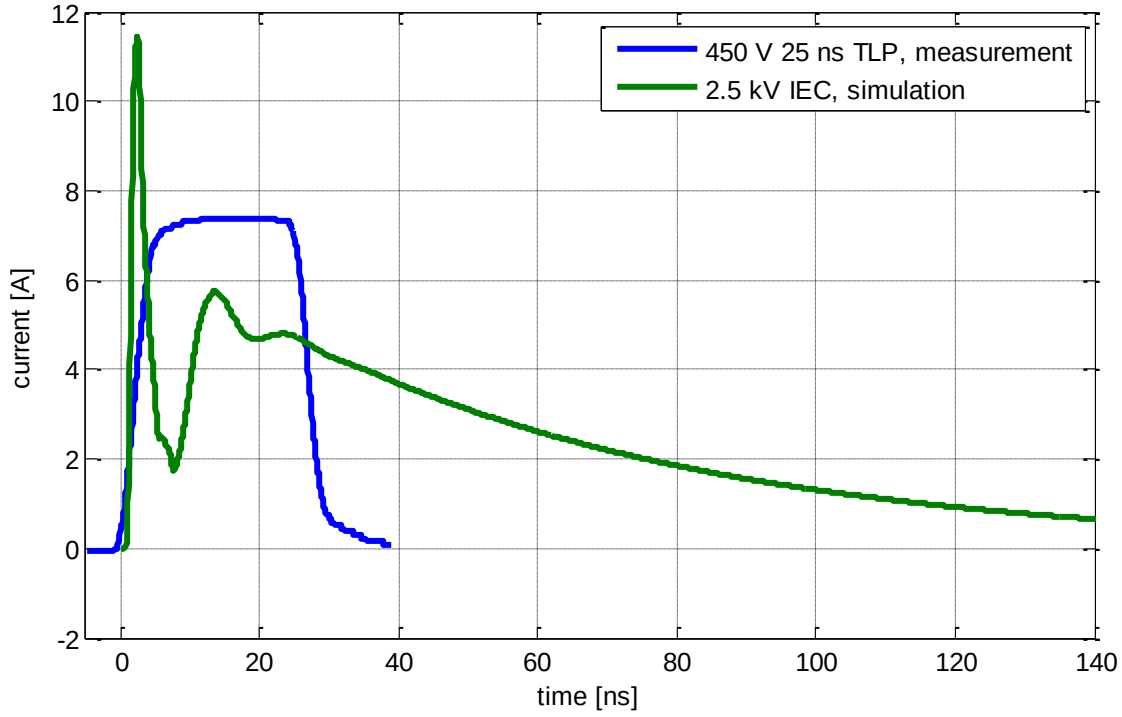

Figure 127: Maximal TLP current and IEC generator current at CANH pin

ESD pulse	V_{ESD} [V]	$V_{IC,max}$ [V]	$I_{IC,max}$ [A]	E_{fail} [µJ]
IEC NoiseKen	2500	100.86	11.44	17.5
TLP 100 ns	250	91.8	3.9	19.2

Table 22: Comparison of IEC and TLP failure energies for CANH pin

4.4.4 **µC DATA**

Measured and simulated waveforms of the discharge current at the connector pin are very similar. In Figure 128 the curves for 5,5 kV charging voltage are presented.

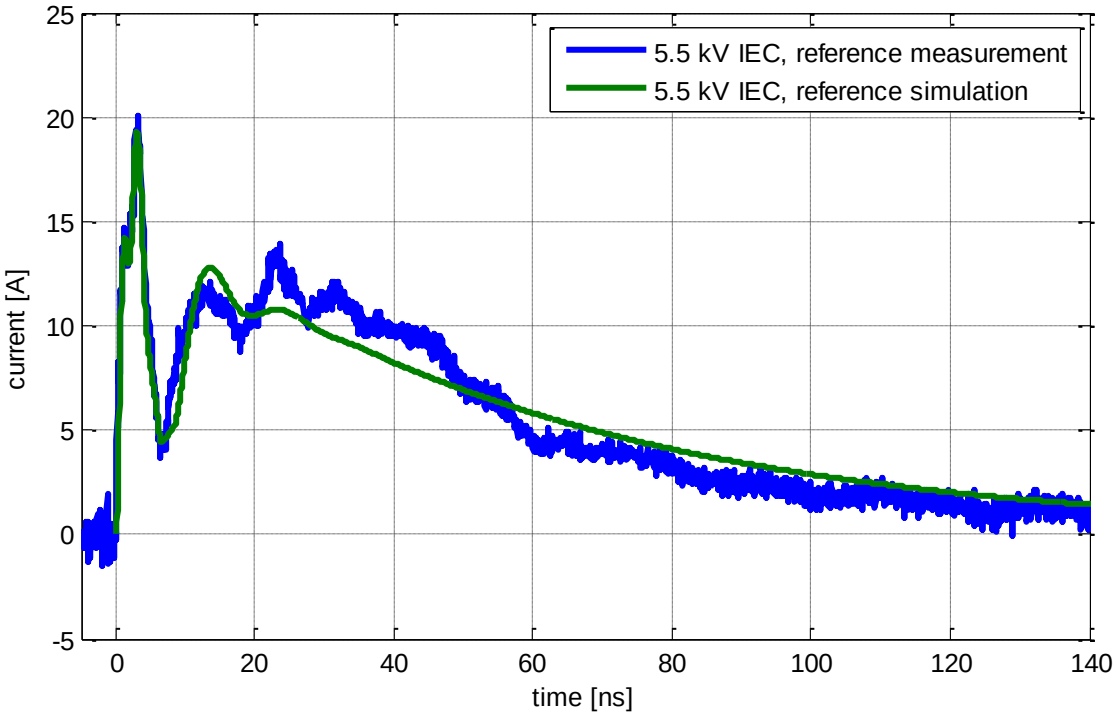

Figure 128: Simulated and measured current for µC DATA pin at connector of demonstrator PCB

In Figure 129 the voltage amplitude measured with the TLP setup increases by factor 3 compared to the IEC amplitude. Maximum TLP charging voltage before destruction was 850 V and pulse width was set to 25 ns. In Table 23 the parameters are compared for the 100 ns TLP measured dataset and the simulated data for the IEC discharge. The deviation between failure energies obtained with both setups is about 9 %. The failure mechanism is also here assumed to be energy-based.

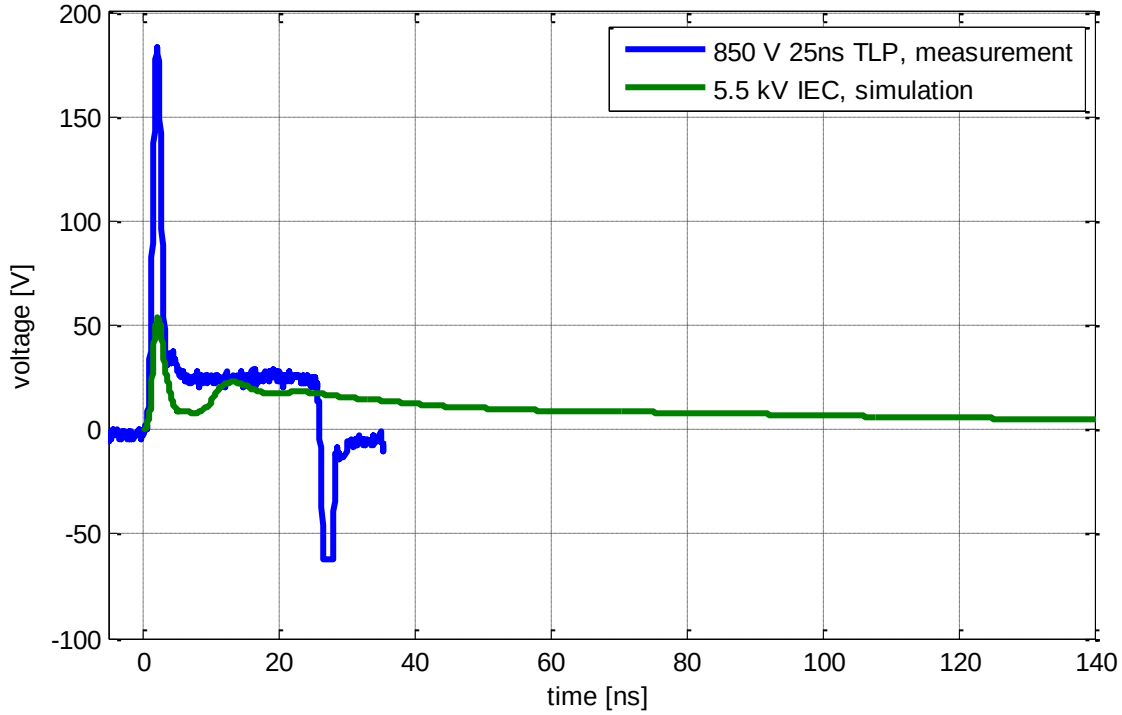

Figure 129: Maximal TLP voltage and IEC generator voltage at µC DATA pin

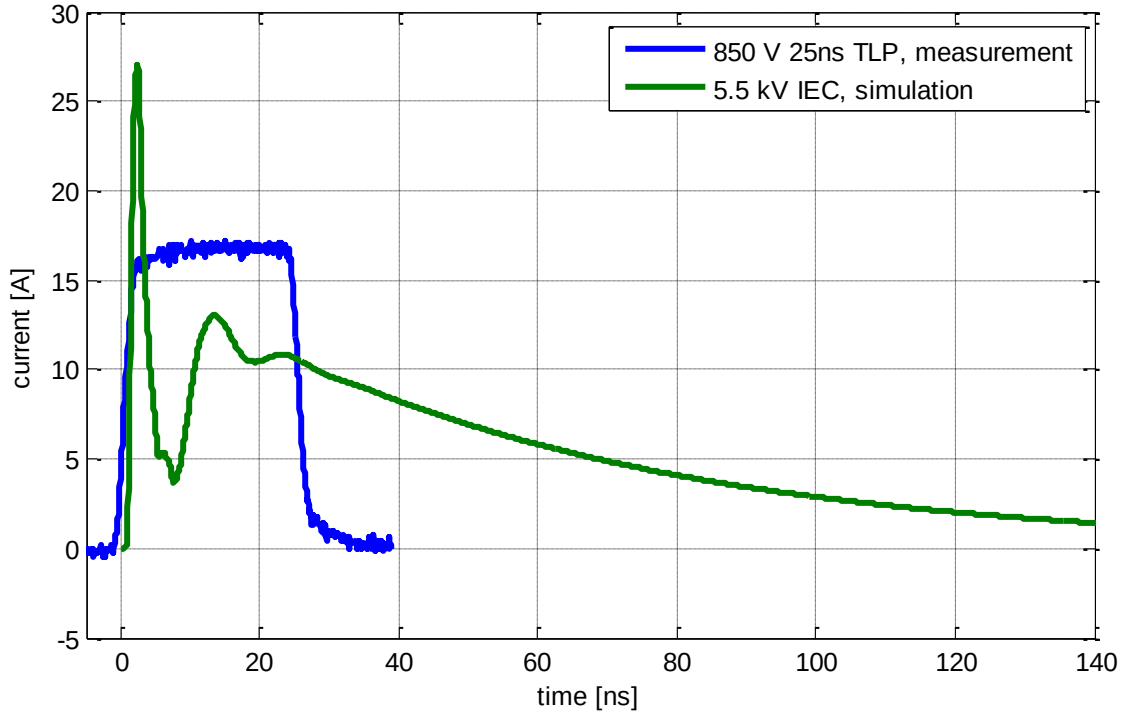

Figure 130: Maximal TLP current and IEC generator current at µC DATA pin

ESD pulse	V_{ESD} [V]	$V_{IC,max}$ [V]	$I_{IC,max}$ [A]	E_{fail} [µJ]
IEC NoiseKen	5500	53.42	27.07	11.30
TLP 100 ns	450	95.4	9.0	12.3

Table 23: Comparison of IEC and TLP failure energies for µC DATA pin

4.4.5 **Measurement results with protection elements**

Similar to the measurement of the IEC failure level without protection devices, the IEC failure levels with ESD protection devices were measured on the demonstrator PCB. A varistor and a TVS diode were investigated. The elements were connected in parallel to the connector pin of the demonstrator PCB. In Figure 131 and Figure 132 the measured and simulated currents for the detected IEC failure level are shown exemplarily for the µC DATA pin.

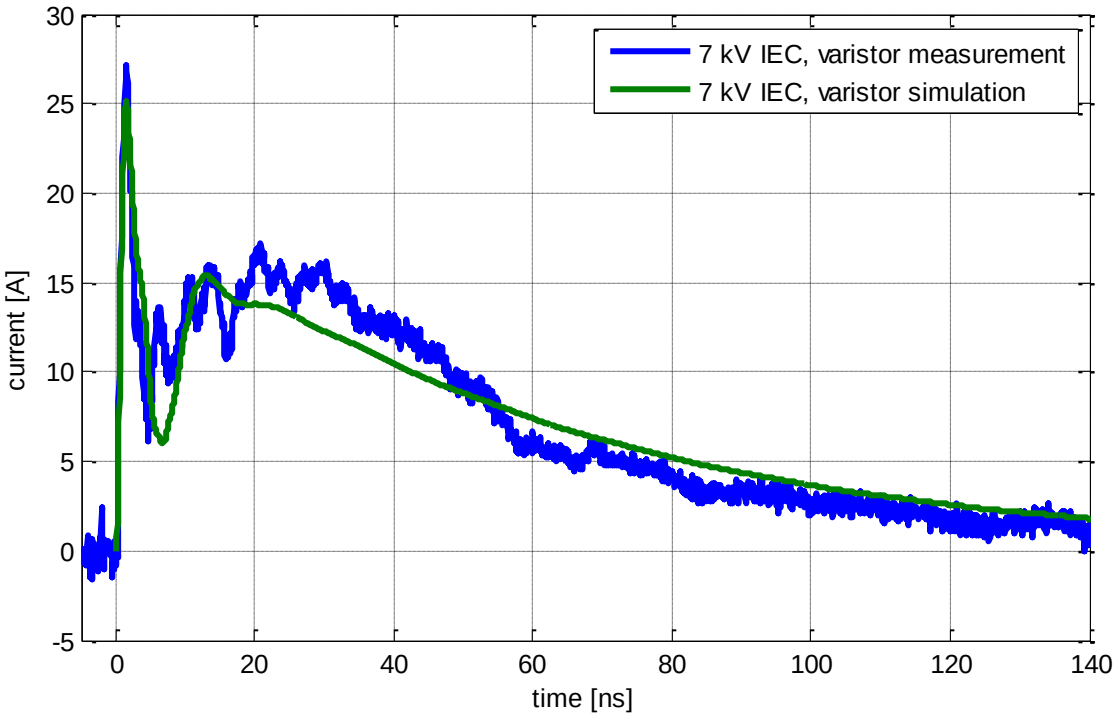

Figure 131: Simulated and measured current for µC DATA pin protected with varistor

Each IC was tested with 3 discharges within 3 seconds for a charging voltage level. After each discharge the IV curve was measured with the source meter. If the current at 2 DC spots did not change, the charging voltage was increased with 0,5 kV or 1 kV steps. The IC failure levels were tested for a minimum of 2 ICs.

Table 24 contains the failure levels obtained for different combinations of IC pins and ESD protection elements. In most cases deviations between measurement and simulation are about 10 %. The maximum deviation is 24 % in case of the TVS diode with very high charging voltages. Destruction was found for the LIN TxD pin at the level of 12 kV charging voltage. Critical temperature of the simulation model is simulated at 9,1 kV charging voltage.

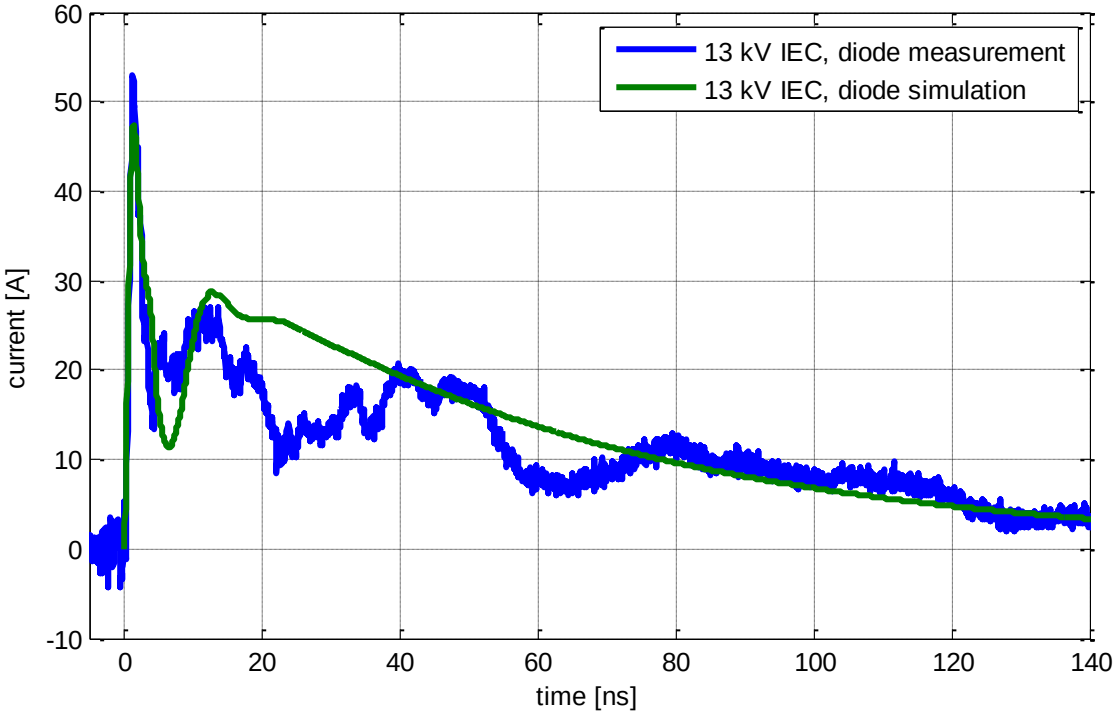

Figure 132: Simulated and measured current for µC DATA pin protected with TVS diode

IC	ESD protection	measurement [kV]	simulation [kV]
LIN-ATA-6662C Atmel TxD pin	No ESD protection	3.0	3.2 **(7%)**
	Varistor EPCOS CT0603K14G	3.5	3.8 **(9%)**
	Diode Protek TVS GBLCS05C	12	9.1 **(24%)**
CAN-TJA1041T NXP CANH pin	No ESD protection	2.5	2.8 **(12%)**
µC-XC864 Infineon DATA pin	No ESD protection	5.5	4.7 **(15%)**
	Varistor EPCOS CT0603K14G	7	7.4 **(6%)**
	Diode Protek TVS GBLCS05C	13	11.5 **(12%)**

Table 24: Comparison of measured and simulated IC ESD failure levels

4.5 Measurement of loop voltage and current

Field coupling on PCB trace loops on the demonstrator PCB is measured. The coupling effect depends on the surface of the loop area and termination impedance.

Two IC pins were selected as real loads because the discharge waveform is affected by the IV characteristic.

4.5.1 **Setup**

The IEC ESD generator was discharged via the connector pin of the demonstrator PCB. Two configurations are considered where the pin is connected to the CAN transceiver CANH pin and to a µC RxD pin. In Figure 133 the shortest distance of the loop to the trace connected to the CANH pin is 2 mm and for the RxD pin 3 mm. The shortest diameter of the loop is 6 mm. The maximum diameter is about 10 cm. The coupled voltage and current signal was measured with an oscilloscope. A current sensor was connected to the SMA connector shown on the picture to measure the loop current. The loop is terminated with 50 Ω impedance from the instrument.

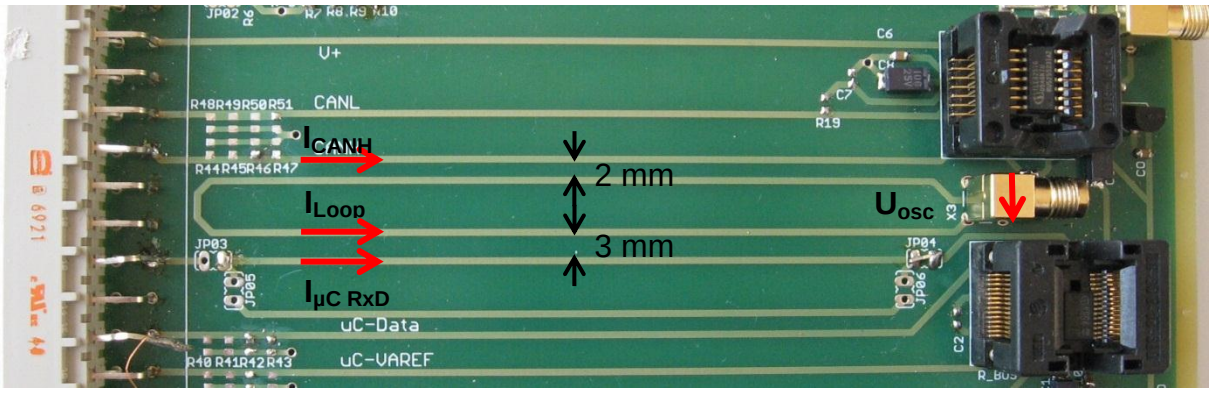

Figure 133: Loop section on demonstrator PCB

4.5.2 **Measurement results**

The measurement results are presented for each configuration. In section 4.5.2.3 waveforms and energies are compared.

4.5.2.1 Discharge into µC RxD pin

Figure 134 shows two measured current waveforms of the 1 kV IEC discharge. The waveforms are very similar for various discharges. The coupled signals are shown in Figure 135 and Figure 136. Similar rise times as measured for the original signal are obtained. The maximum amplitudes are 8 V and about 175 mA. The coupling factor between the current through IC pin and the coupling signal in the loop is about 21.

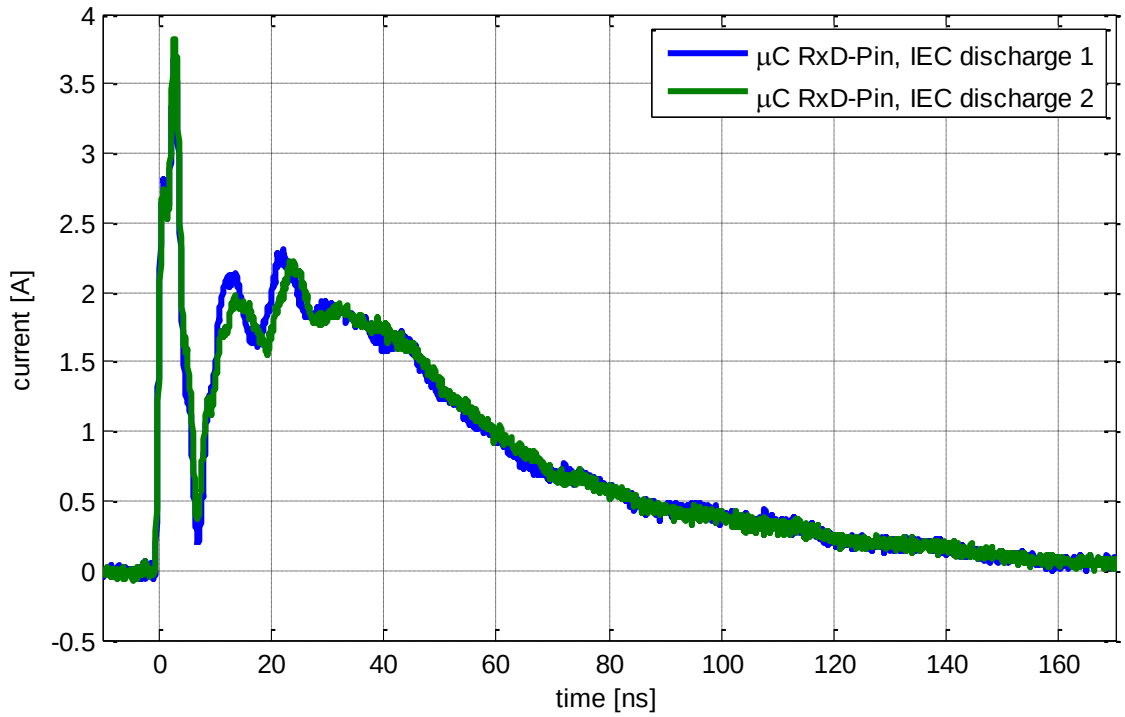

Figure 134: Current of 1 kV IEC generator discharge into µC RxD pin

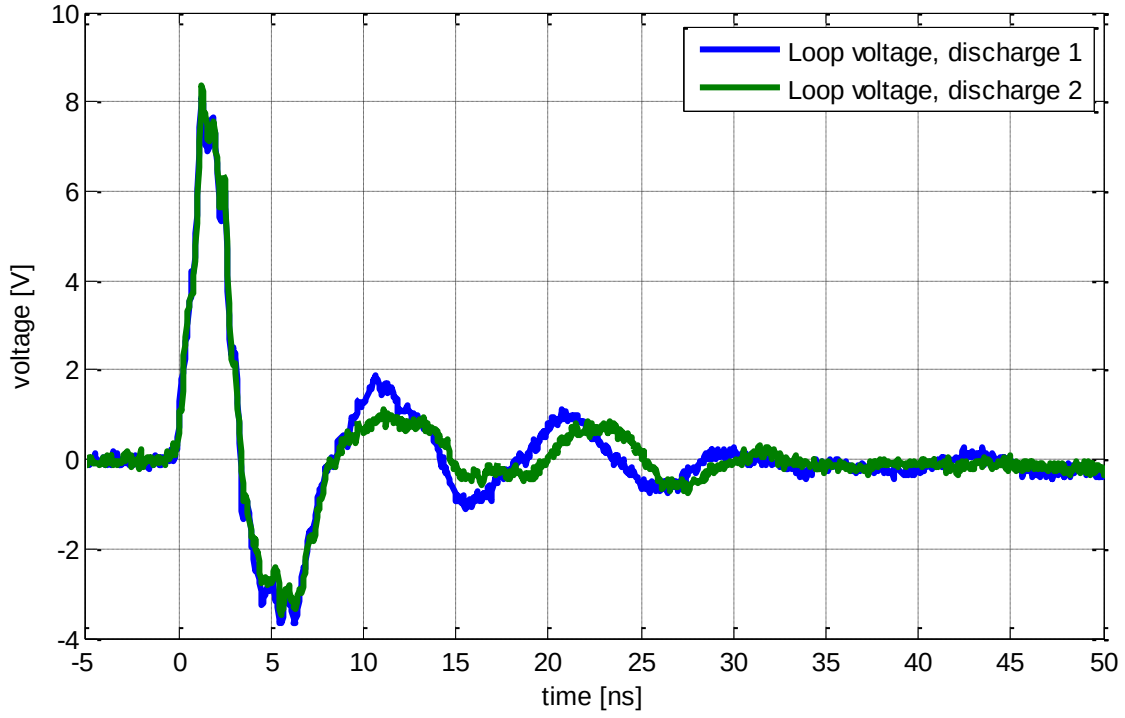

Figure 135: Measured loop voltage over 50 Ω for discharge into µC RxD pin

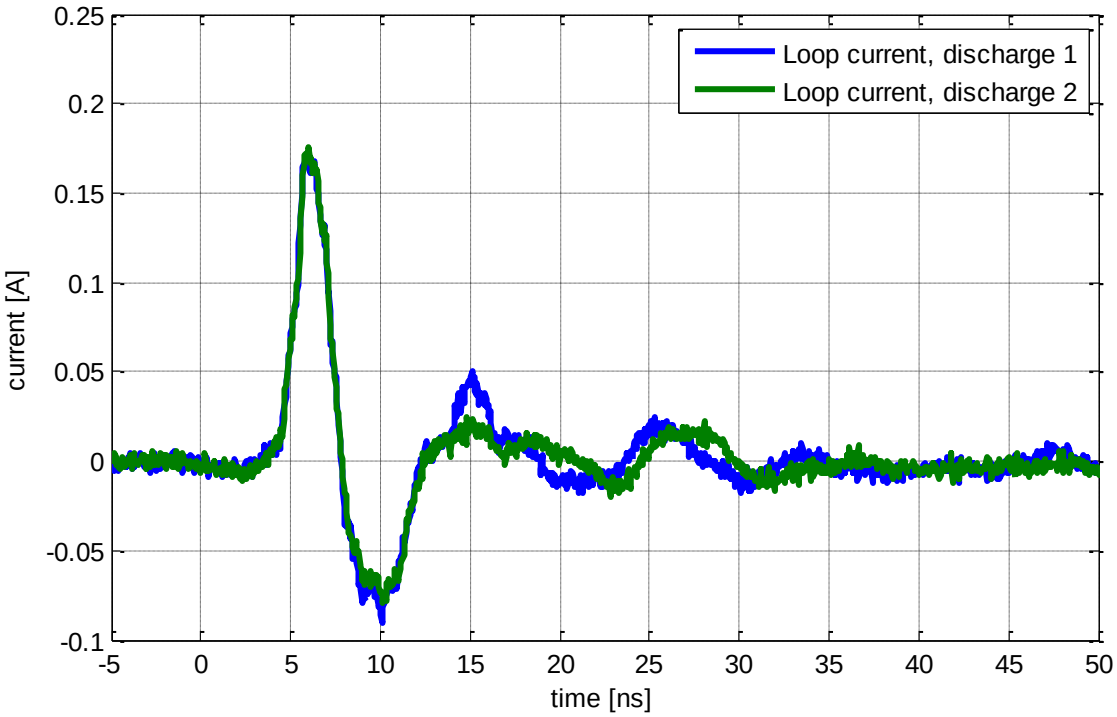

Figure 136: Measured loop current for discharge into µC RxD pin

4.5.2.2 Discharge into CANH pin

Similar signals are obtained if the IEC generator is discharged into the conductor connected to the CANH pin. Figure 137 to Figure 139 show that the waveforms are stable. Coupling pulse shape is inverted because the pulse source was discharged at the opposite side of the loop compared to the discharge to the RxD pin, but the direction of the current flow remains the same.

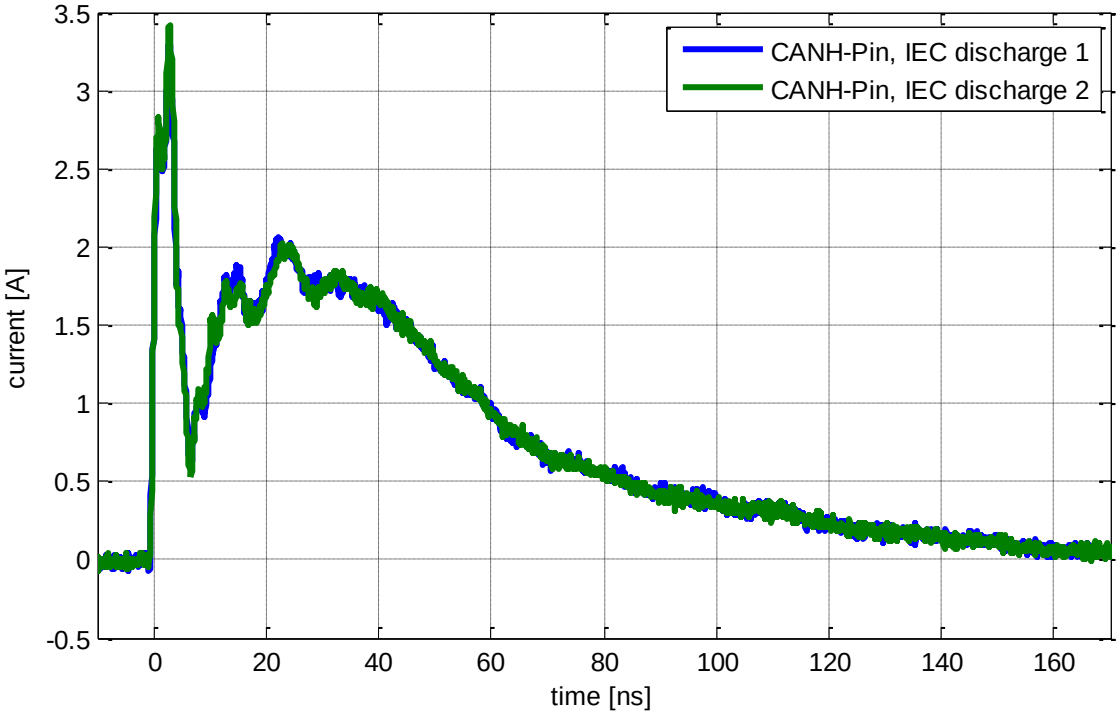

Figure 137: Current of 1 kV IEC generator discharge into CANH pin

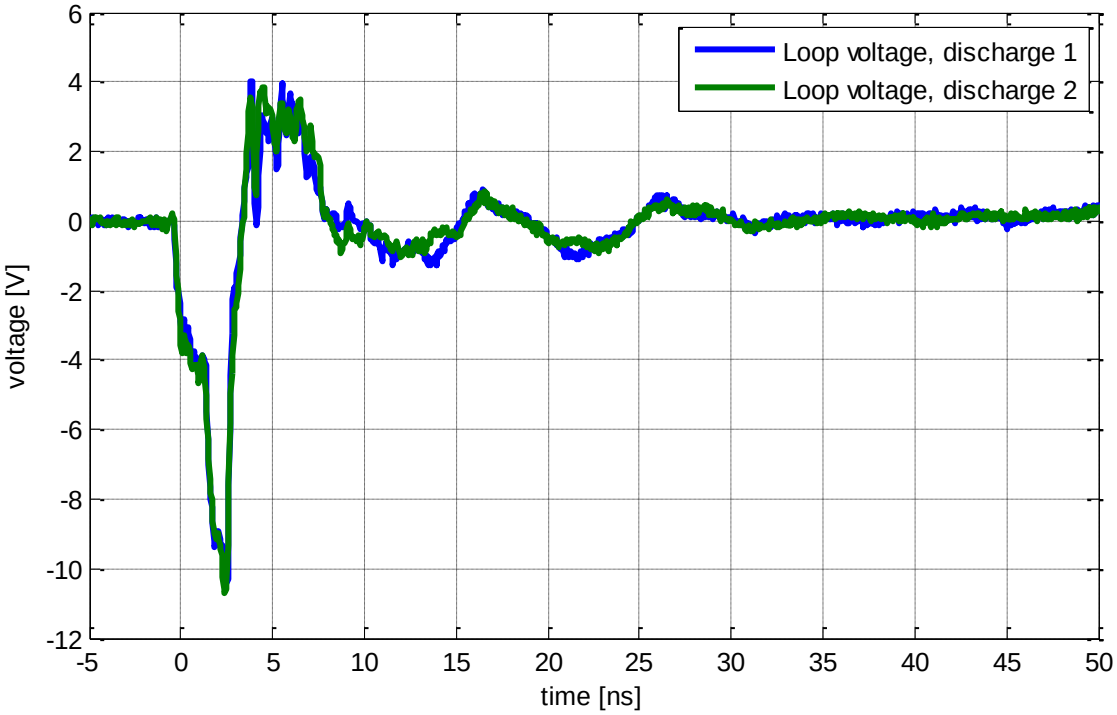

Figure 138: Measured loop voltage over 50 Ω for discharge into CANH pin

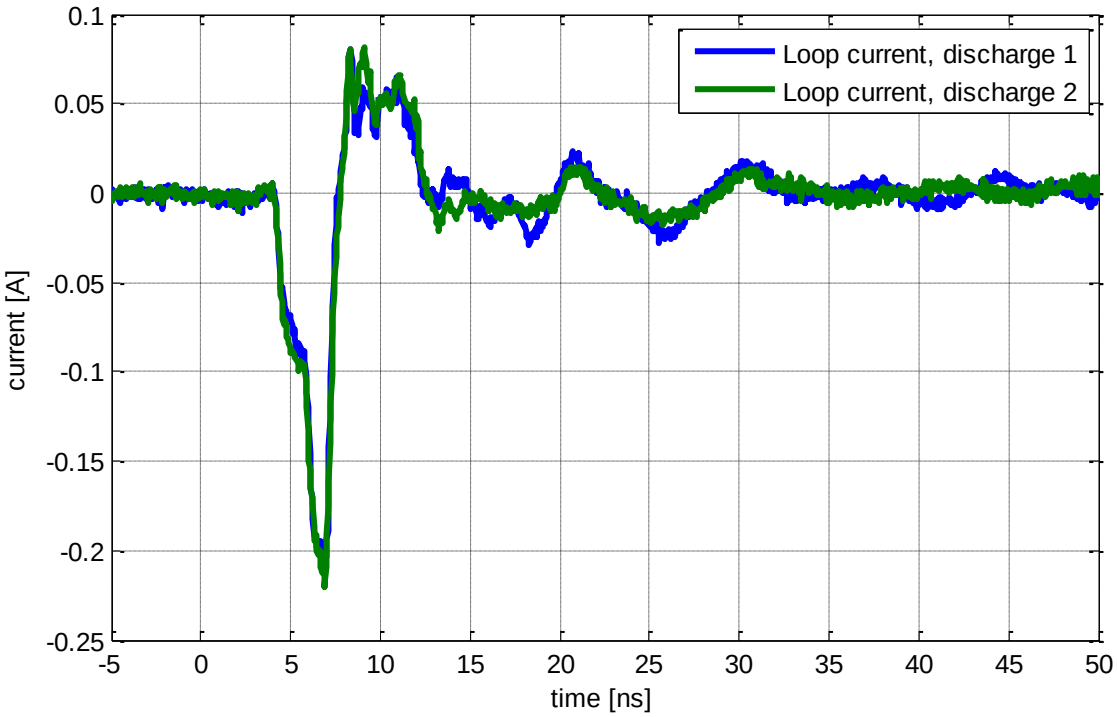

Figure 139: Measured loop current for discharge into CANH pin

4.5.2.3 Comparison of measured data for discharges into CANH pin and µC pin

The distance between the traces is shorter if the IEC generator is discharged via the conductor connected to the CANH pin. In Figure 141 and Figure 142 the µC RxD waveforms were multiplied by - 1 for comparison. According to Figure 140 a smaller current amplitude was measured for the discharge into the CANH pin but coupling peak amplitudes in the loop are higher. After Table 25 the deviation between the coupling energies for both configurations is low. For a 1 kV IEC discharge only about 1,3 nJ were measured.

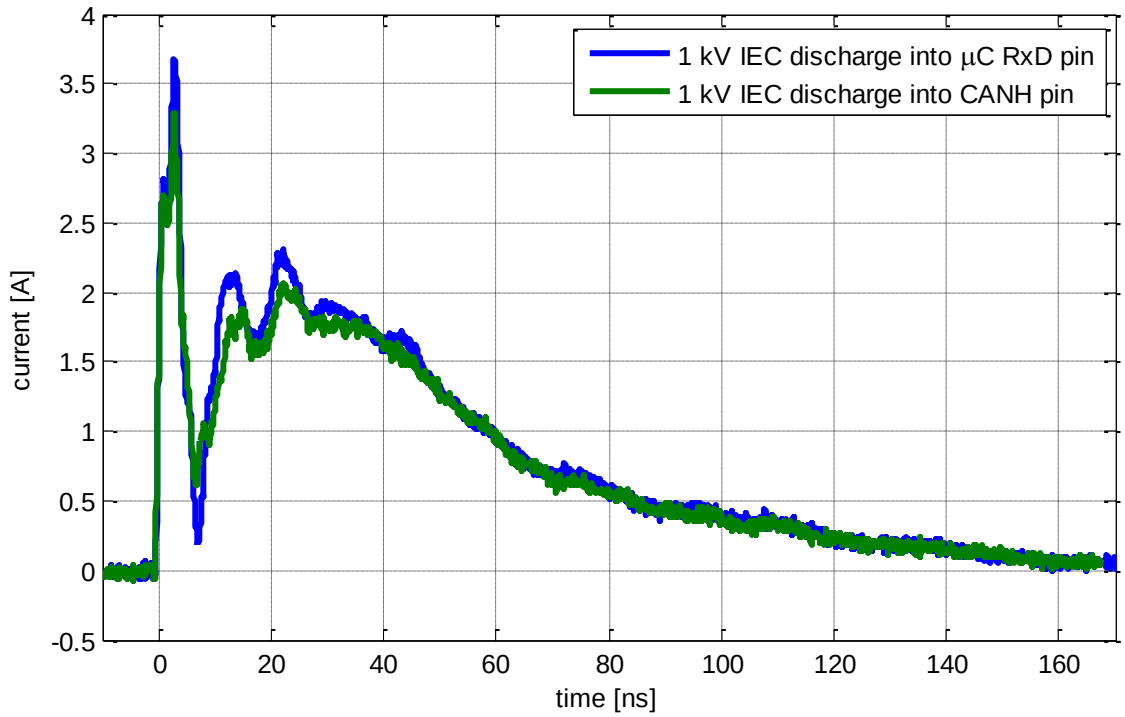

Figure 140: Comparison of measured currents for 1 kV IEC discharge

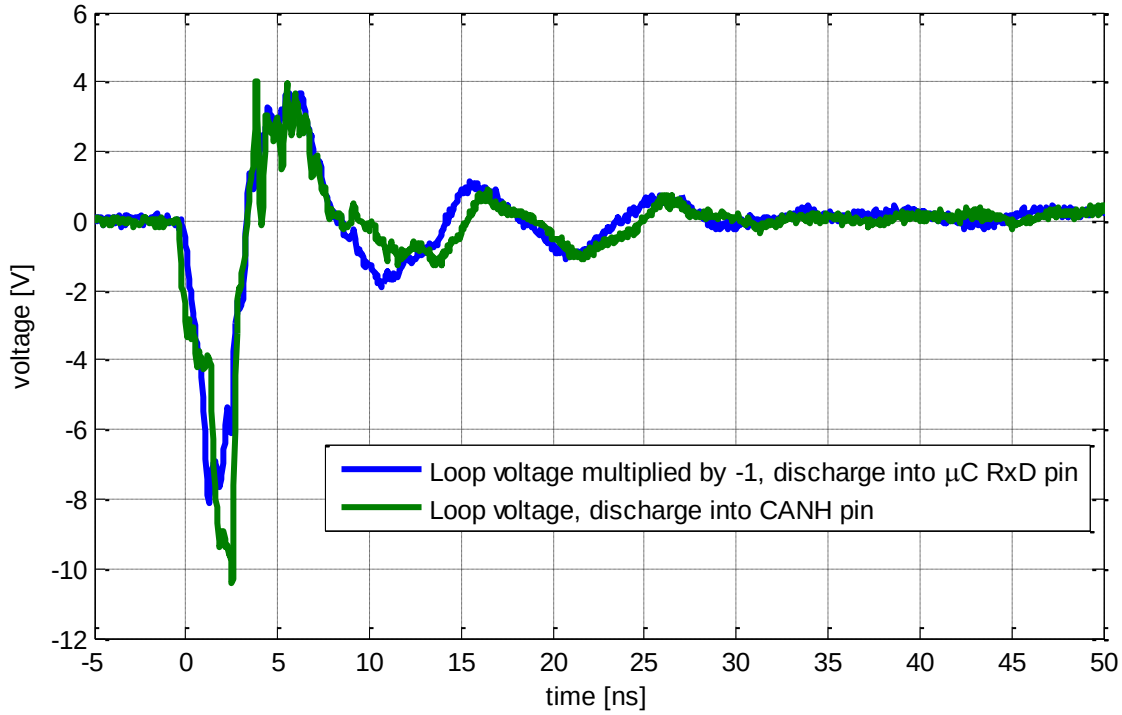

Figure 141: Comparison of measured loop voltages

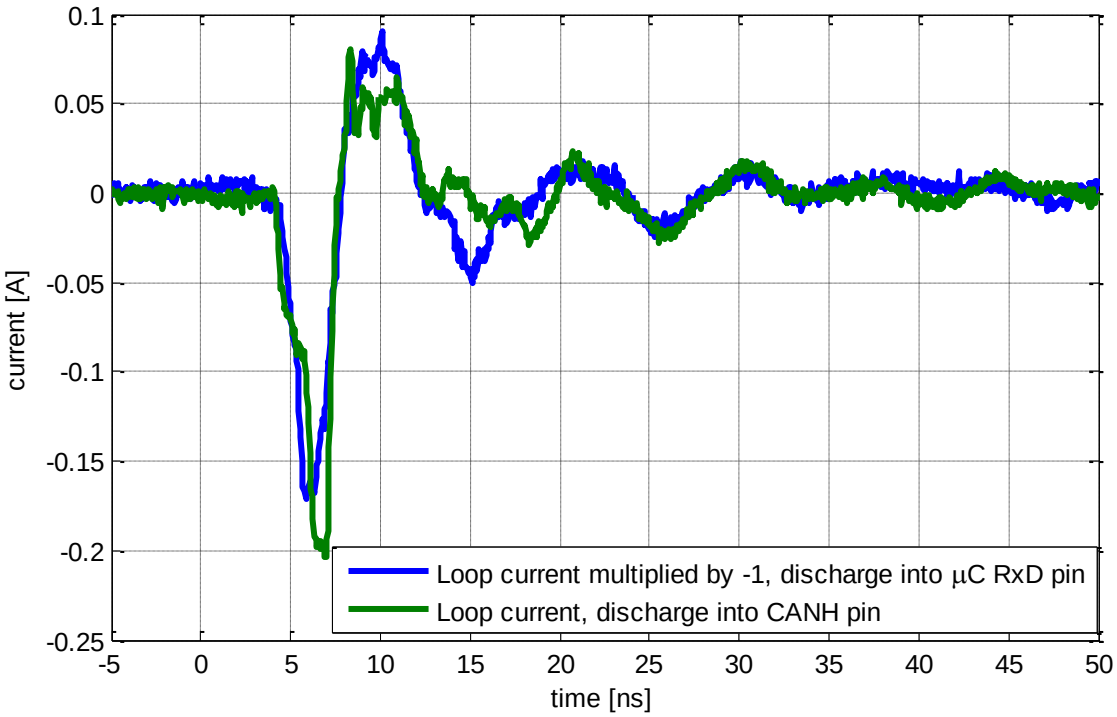

Figure 142: Comparison of measured loop currents

Load	Discharge 1 measured loop energy	Discharge 2 measured loop energy
CANH	1,18 nJ	1.37 nJ
µC RxD Pin	1.50 nJ	1.30 nJ

Table 25: Comparison of measured loop energies for 1 kV IEC generator discharges into ICs

5 Simulation results

In chapter 4 simulation results and models of different configurations were verified by measurement. The analysis of the impact of a reduction of the HBM ESD robustness of local pins is done based on simulation results.

To estimate the comparability of pulse sources for variable load conditions, voltages and energies are simulated for a fixed PCB conductor configuration in section 5.1. Section 5.2 deals with the impact of the charging voltage on coupled signals. PCB traces are terminated with resistors and IC models.

In section 5.3 to 0 the effect of ESD protection elements on different configurations is analyzed. The impact of PCB parameters on ESD coupling is described in section 5.7 on the example of coupling energies. The results of problematic configurations are presented in section 5.8.

5.1 Simulation of coupled signals for different load conditions

The disturbance of ICs by coupling from ESD events can be described in terms of coupled curve shapes of voltage and current waveforms and energy dissipated in an IC. In this section the coupling effects with different configurations are analyzed. For investigation a conductor arrangement like the cross-talk section on the demonstrator PCB is implemented in VHDL-AMS. A lossy transmission line model with three conductors was used.

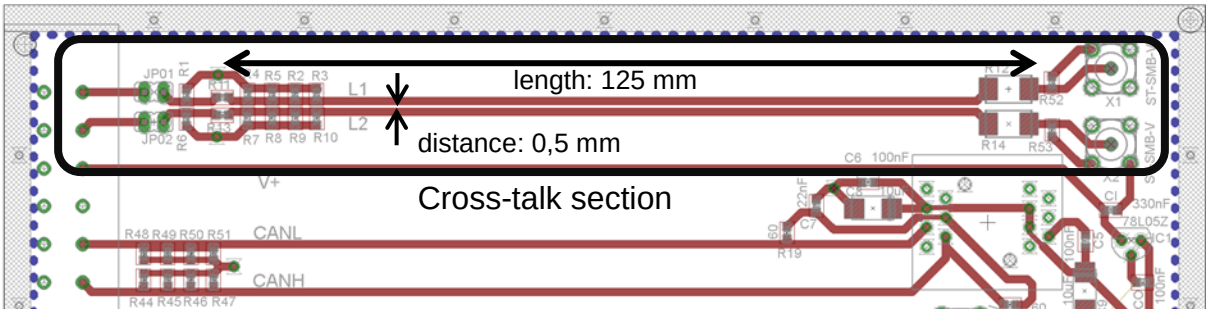

Figure 143: Simulation setup with reference to cross-talk section of the demonstrator PCB

The common mode and differential mode impedances for the transmission line model can be calculated by the use of TXLINE [16].

Z_{com} and Z_{diff}, needed as model parameter, are found with the following equations.

$$Z_{com} = \frac{1}{2} \cdot Z_{even} = 77{,}5\Omega$$

$$Z_{diff} = 2 \cdot Z_{odd} = 144{,}1\Omega$$

The waveforms were simulated for three different pulses sources by connecting the IEC generator model, the HBM generator model, and the TLP model described in section 2.1. In Figure 144 a schematic is shown. One end of trace 1 is terminated with the pulse generator model. The second ends of trace 1 is connected via the

impedance Z to ground. Also both ends of the parallel trace 2 are connected to ground with impedances Z. The configuration is simulated applying different values for Z:

- 1 Ω
- 10 Ω
- 100 Ω
- 1 kΩ
- 10 kΩ

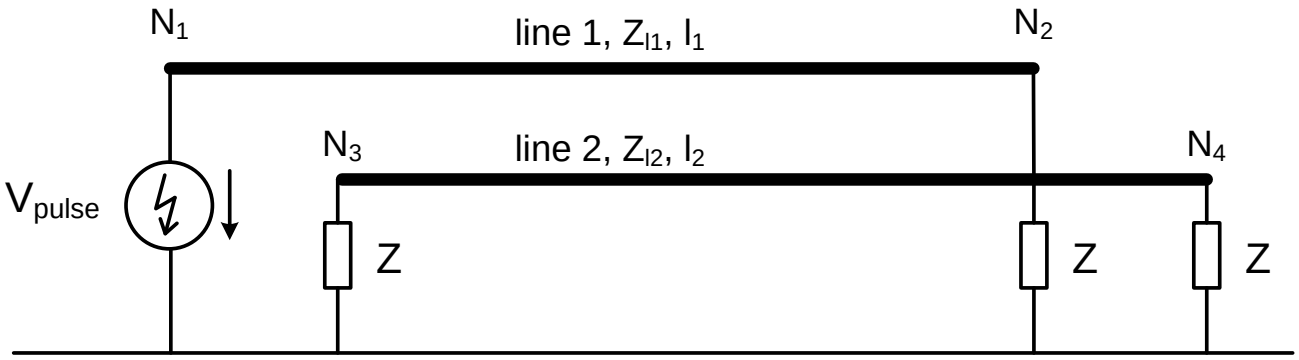

Figure 144: Setup for simulation of coupling effects

All simulated waveforms on node N2 and node N4 according to Figure 144 are shown in the following sections. Waveforms were simulated with two different charging voltages. 1 kV was selected for the IEC and TLP generator. HBM generator charging voltage was set to 2 kV as the common IC robustness level.

Energies and maximum voltage amplitudes are analyzed.

5.1.1 Simulated waveforms for Z = 1 Ω

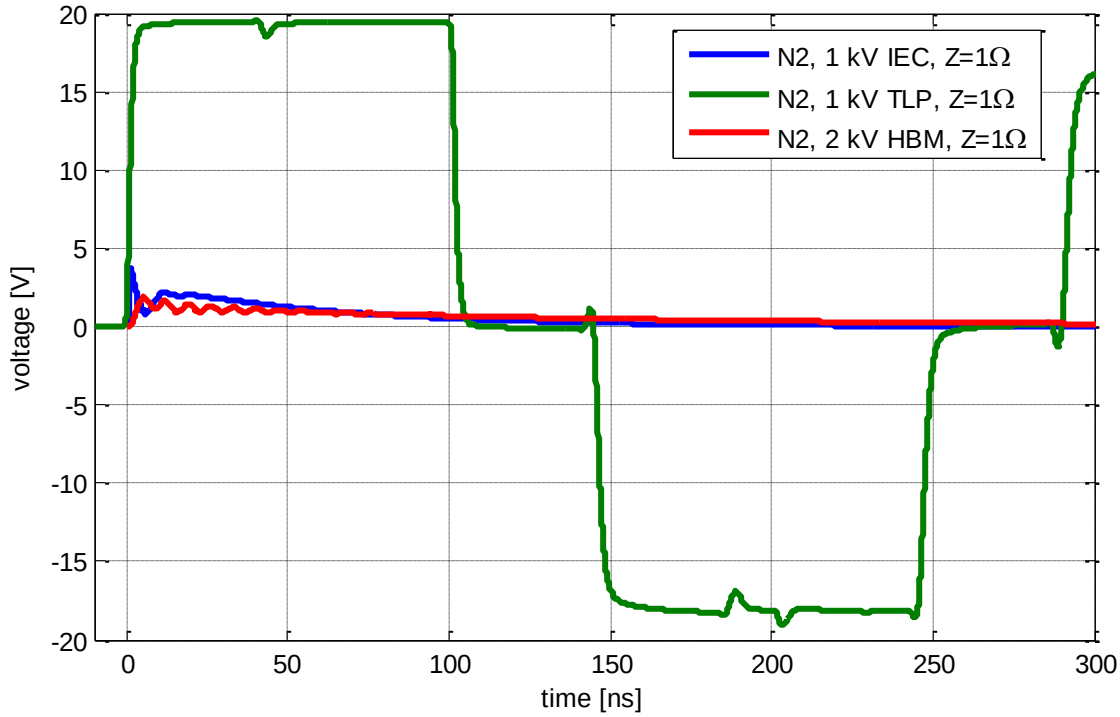

Figure 145: Simulated voltage at node 2 for Z = 1 Ω

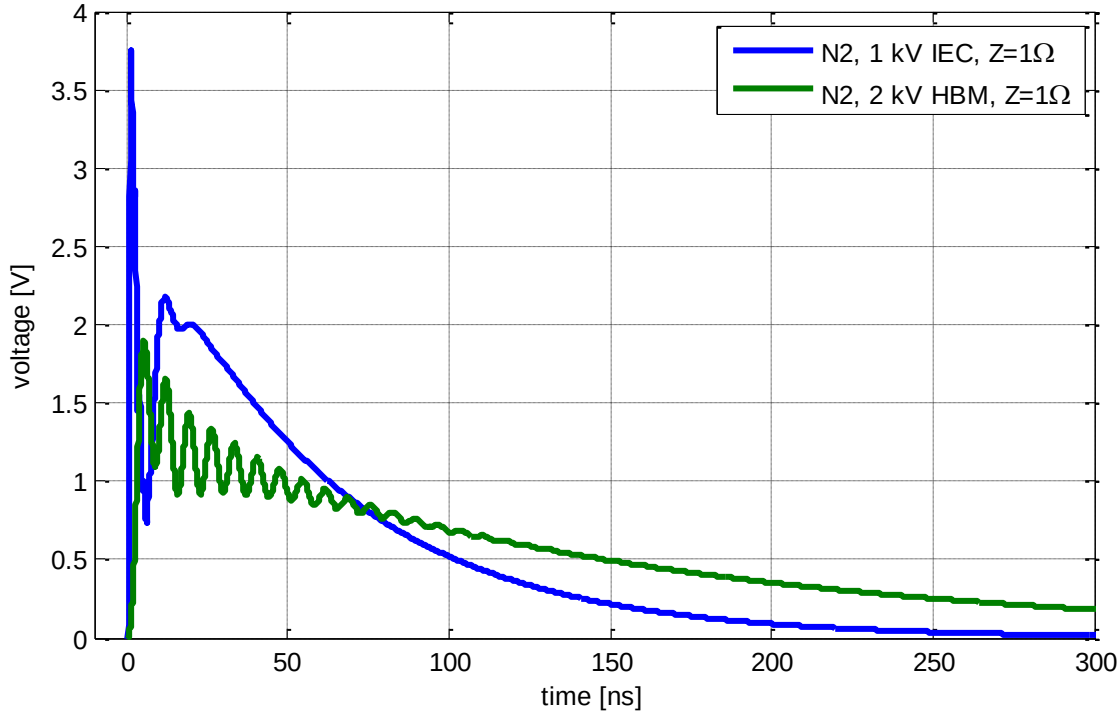

Figure 146: Simulated voltage of an IEC and HBM discharge at node 2 for Z = 1 Ω

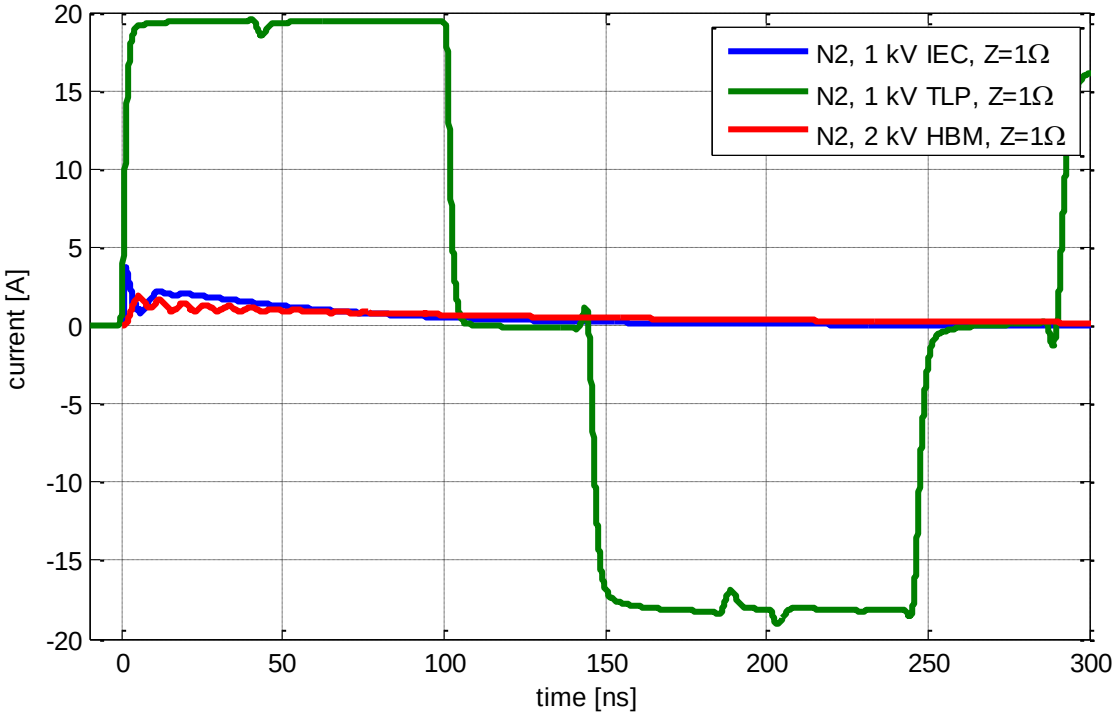

Figure 147: Simulated current at node 2 for Z = 1 Ω

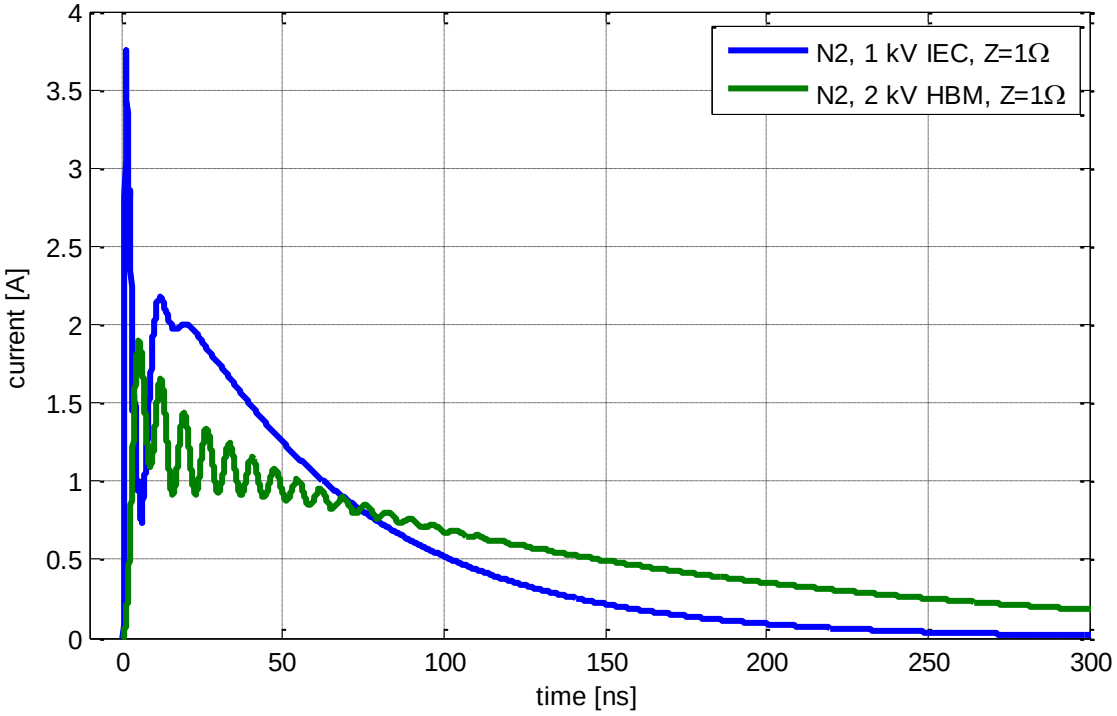

Figure 148: Simulated current of an IEC and HBM discharge at node 2 for Z = 1 Ω

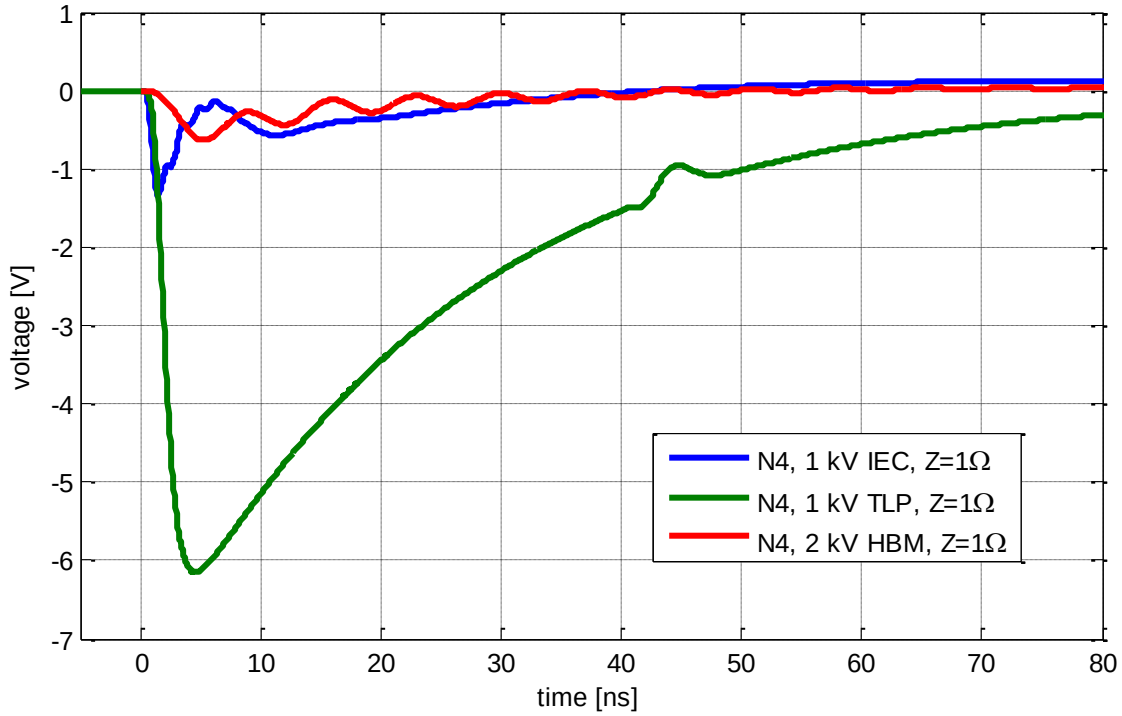

Figure 149: Simulated voltage at node 4 for Z = 1 Ω

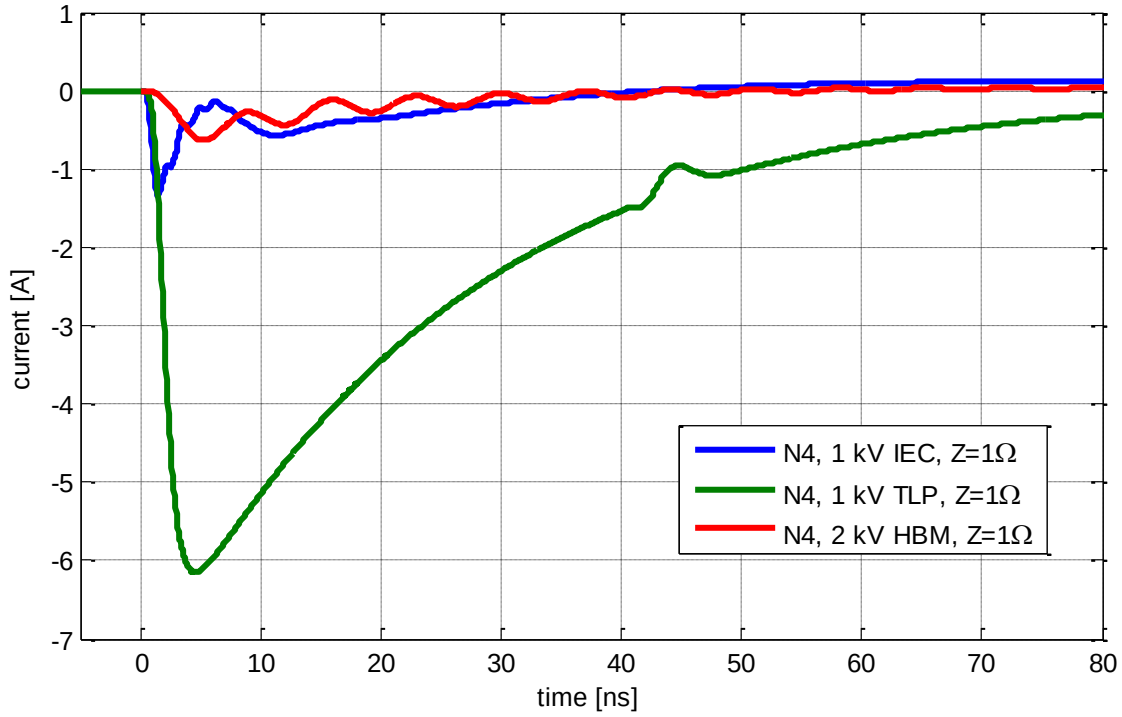

Figure 150: Simulated current at node 4 for Z = 1 Ω

5.1.2 **Simulated waveforms for Z = 10 Ω**

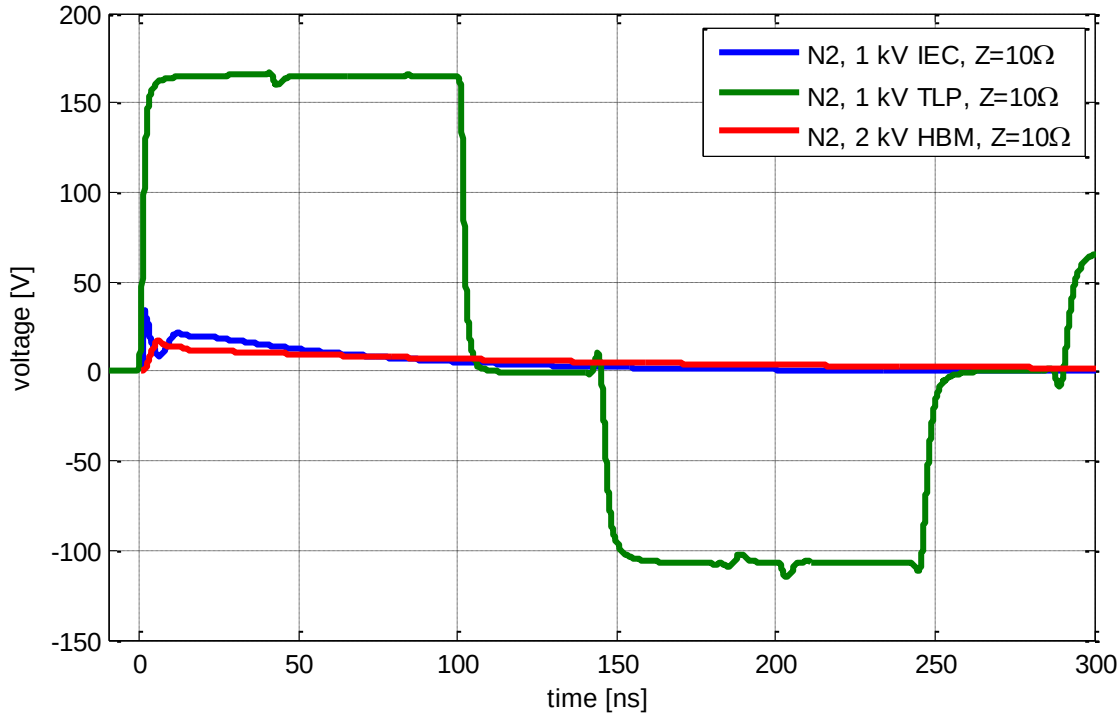

Figure 151: Simulated voltage at node 2 for Z = 10 Ω

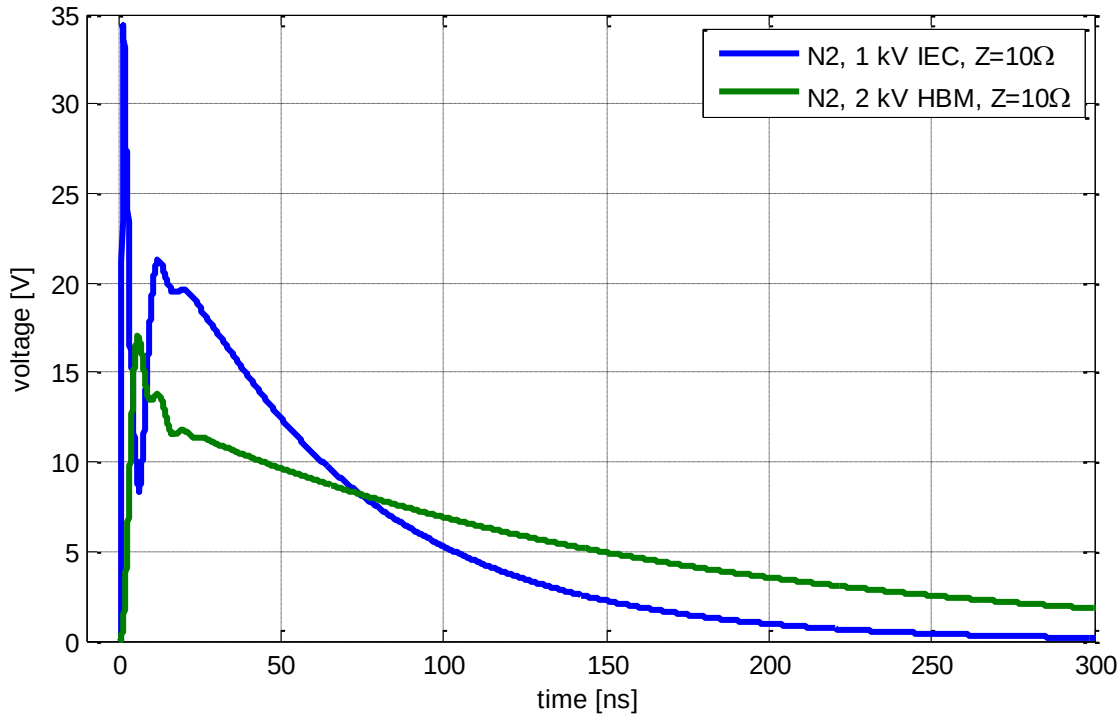

Figure 152: Simulated voltage of an IEC and HBM discharge at node 2 for Z = 10 Ω

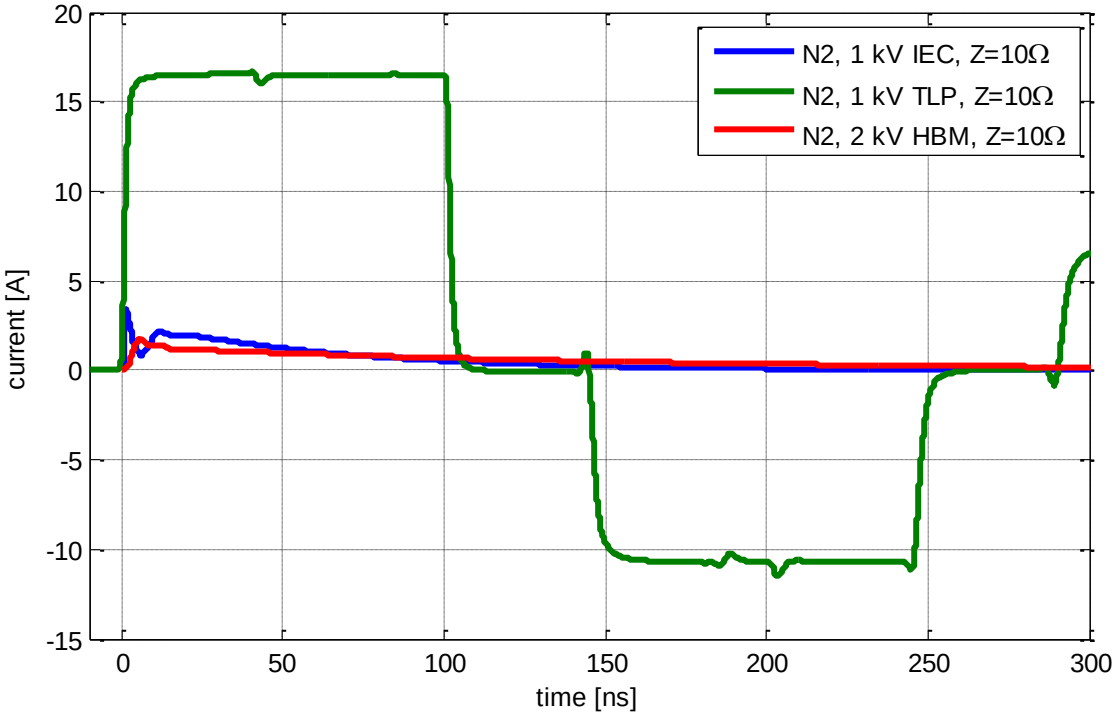

Figure 153: Simulated current at node 2 for Z = 10 Ω

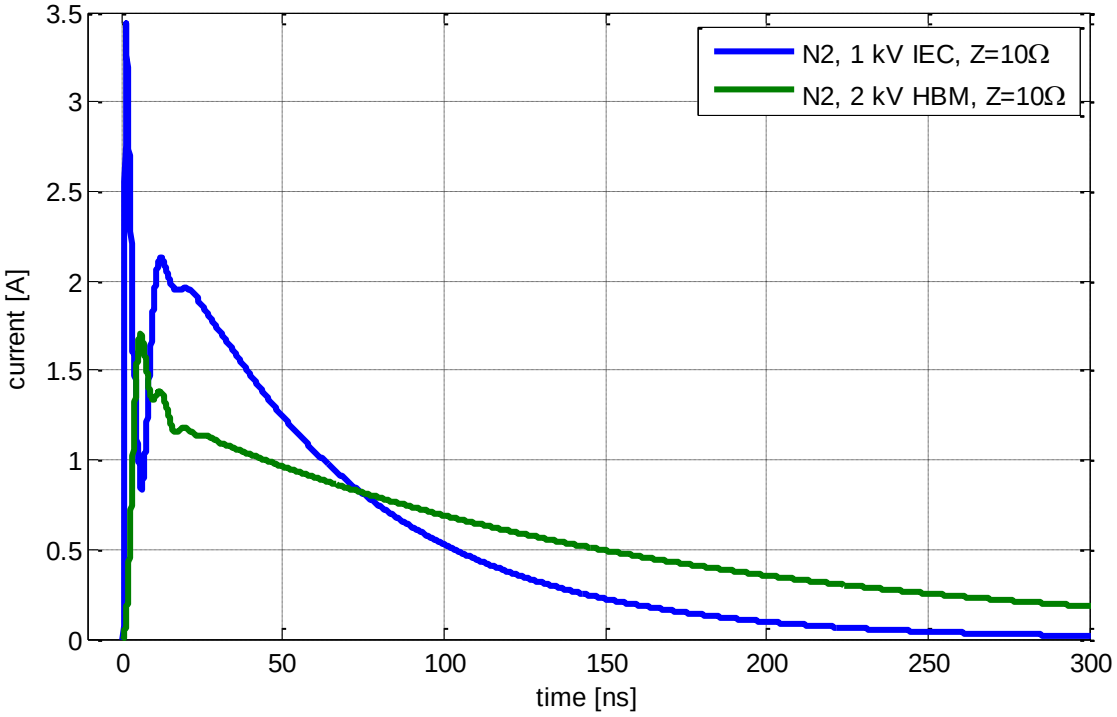

Figure 154: Simulated current of an IEC and HBM discharge at node 2 for Z = 10 Ω

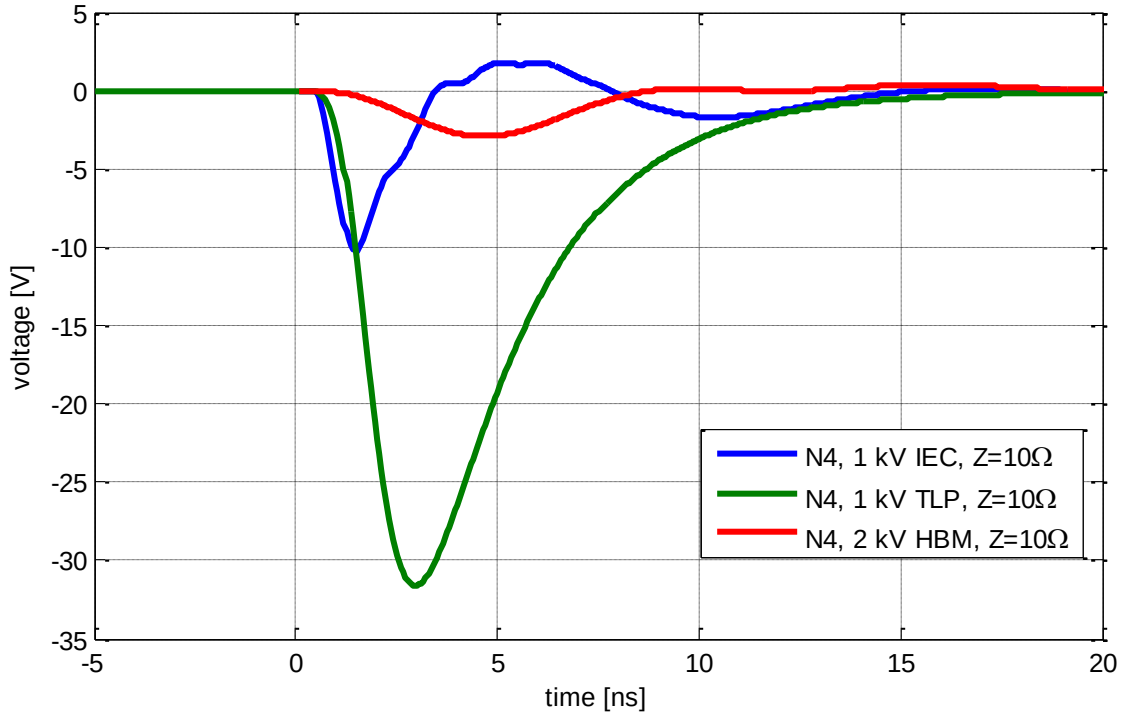

Figure 155: Simulated voltage at node 4 for Z = 10 Ω

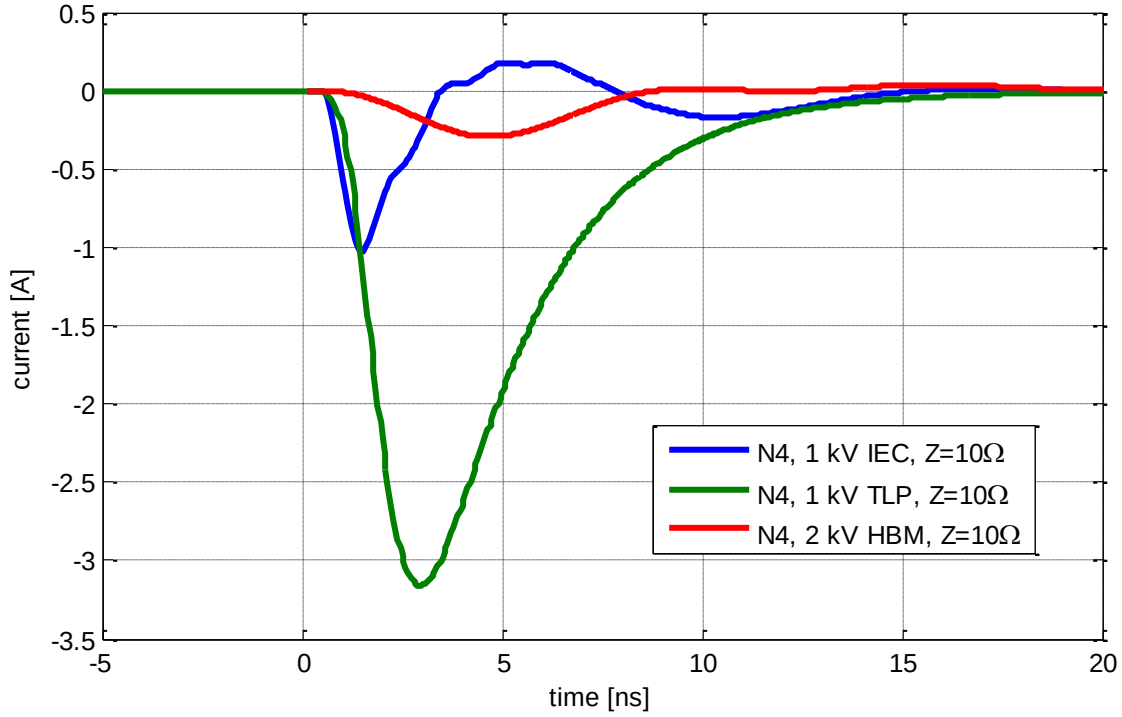

Figure 156: Simulated current at node 4 for Z = 10 Ω

5.1.3 **Simulated waveforms for Z = 100 Ω**

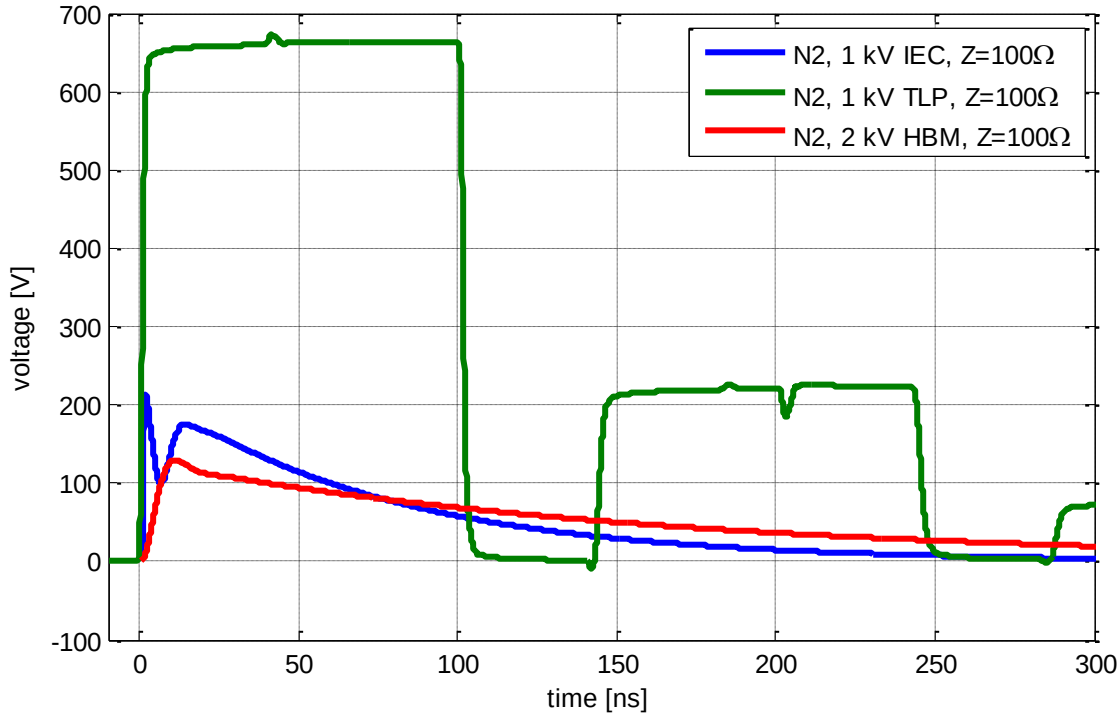

Figure 157: Simulated voltage at node 2 for Z = 100 Ω

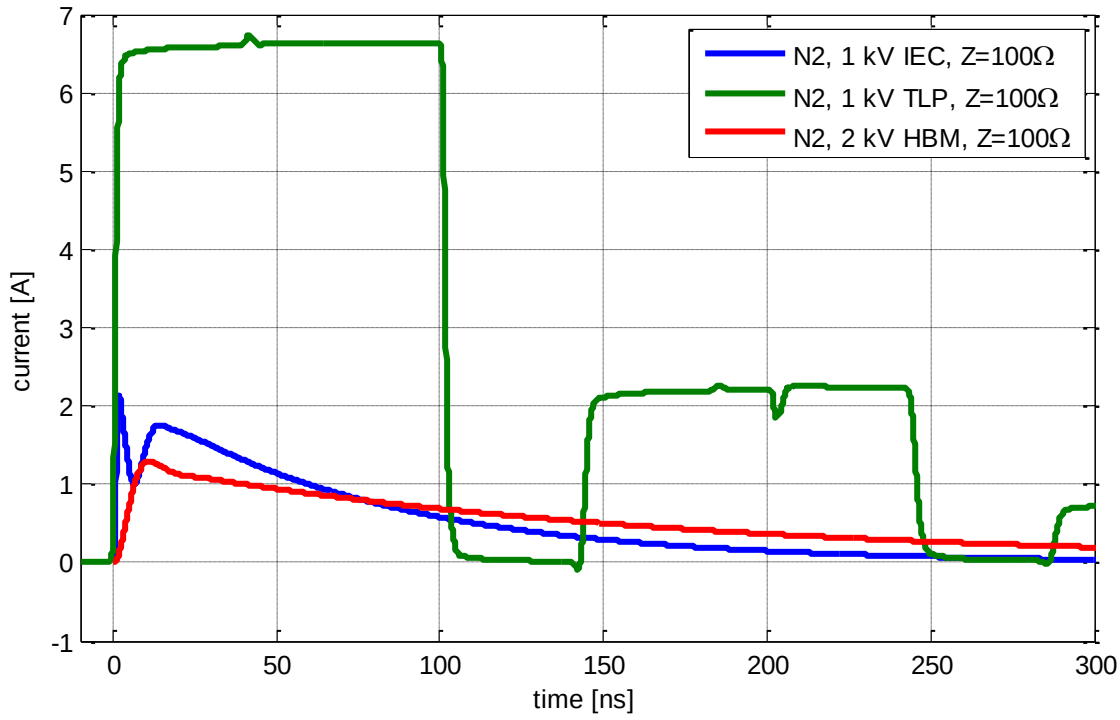

Figure 158: Simulated current at node 2 for Z = 100 Ω

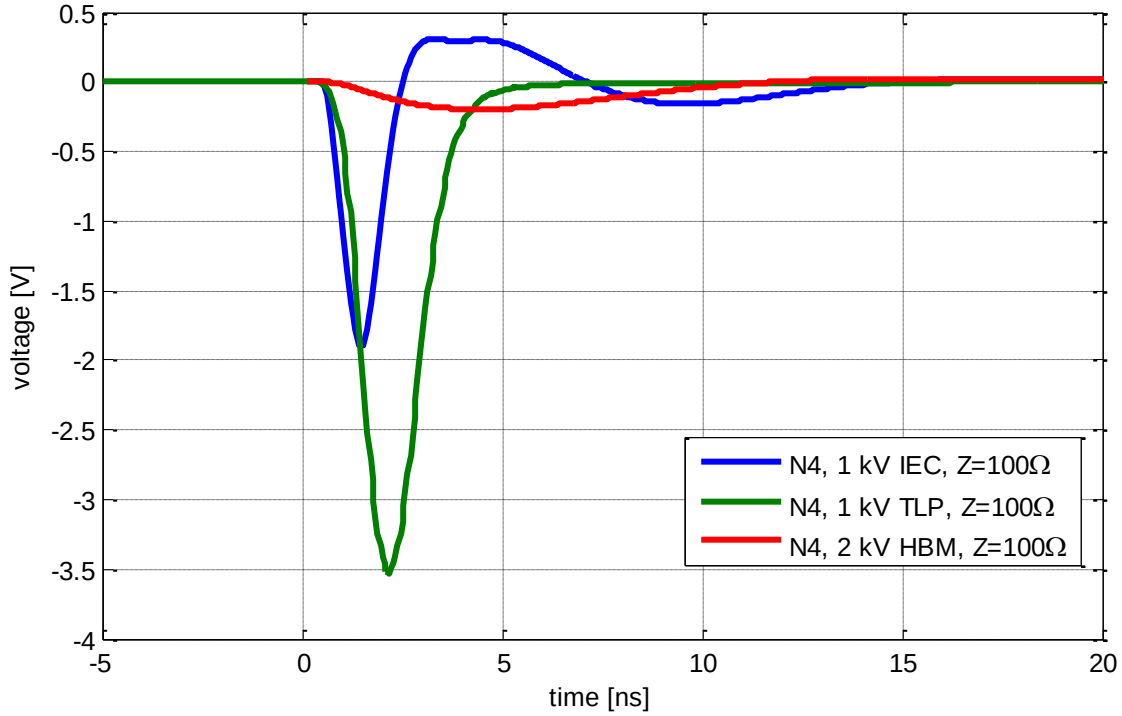

Figure 159: Simulated voltage at node 4 for Z = 100 Ω

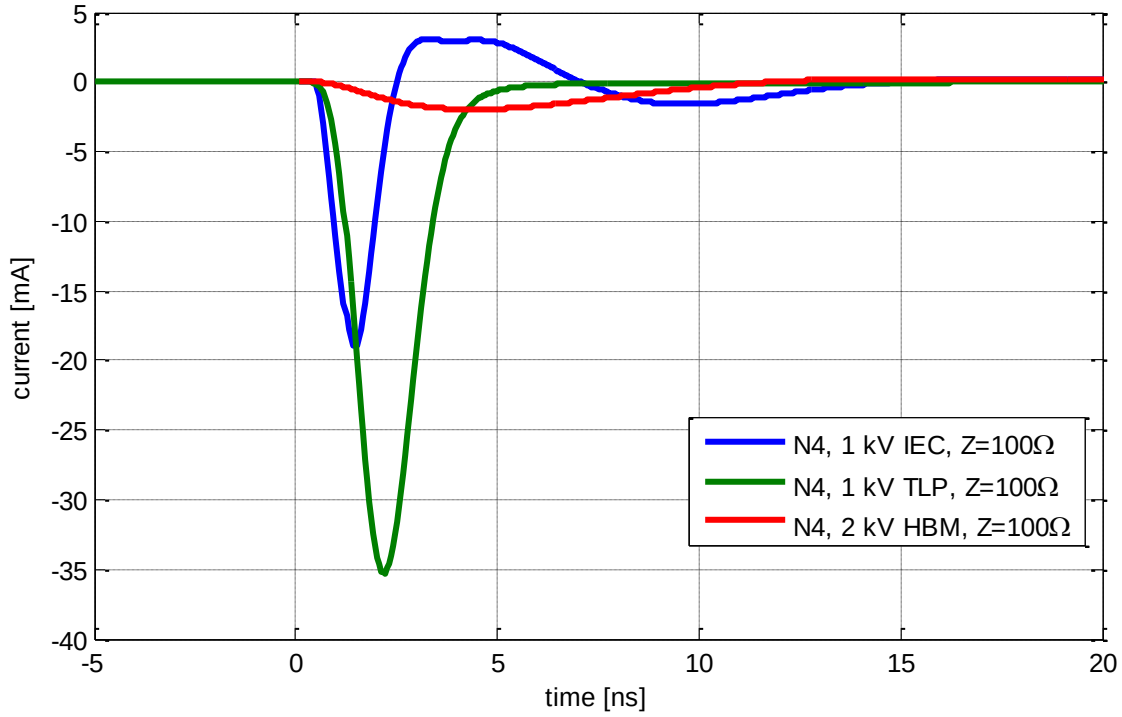

Figure 160: Simulated current at node 4 for Z = 100 Ω

5.1.4 **Simulated waveforms for Z = 1 kΩ**

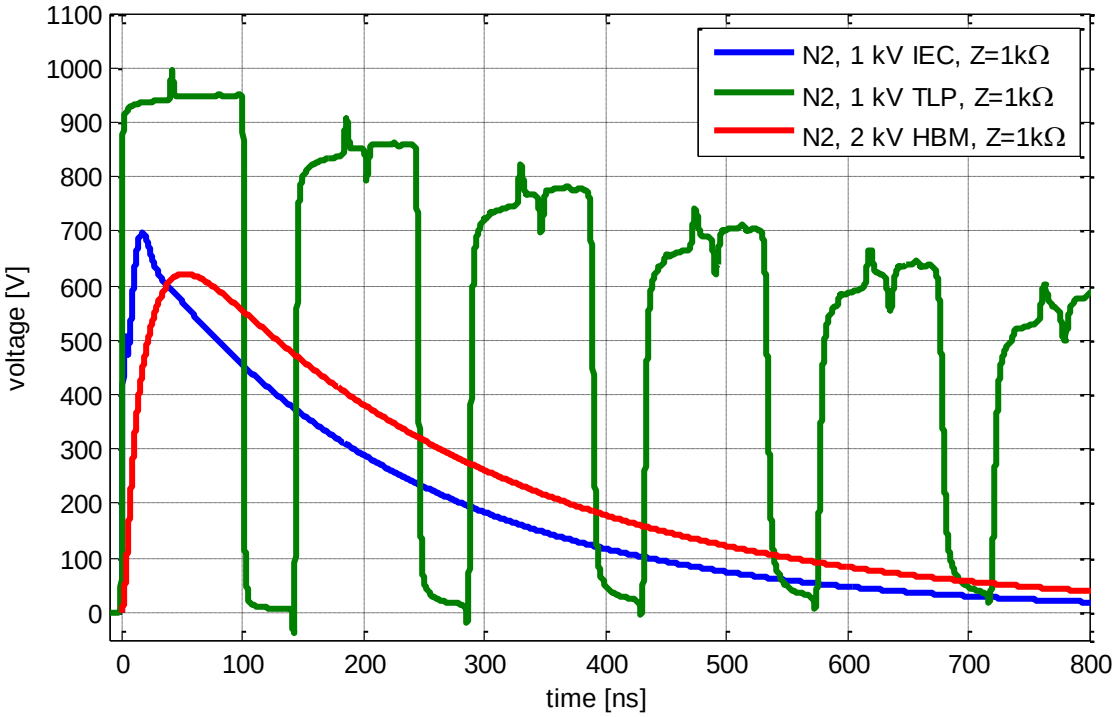

Figure 161: Simulated voltage at node 2 for Z = 1 kΩ

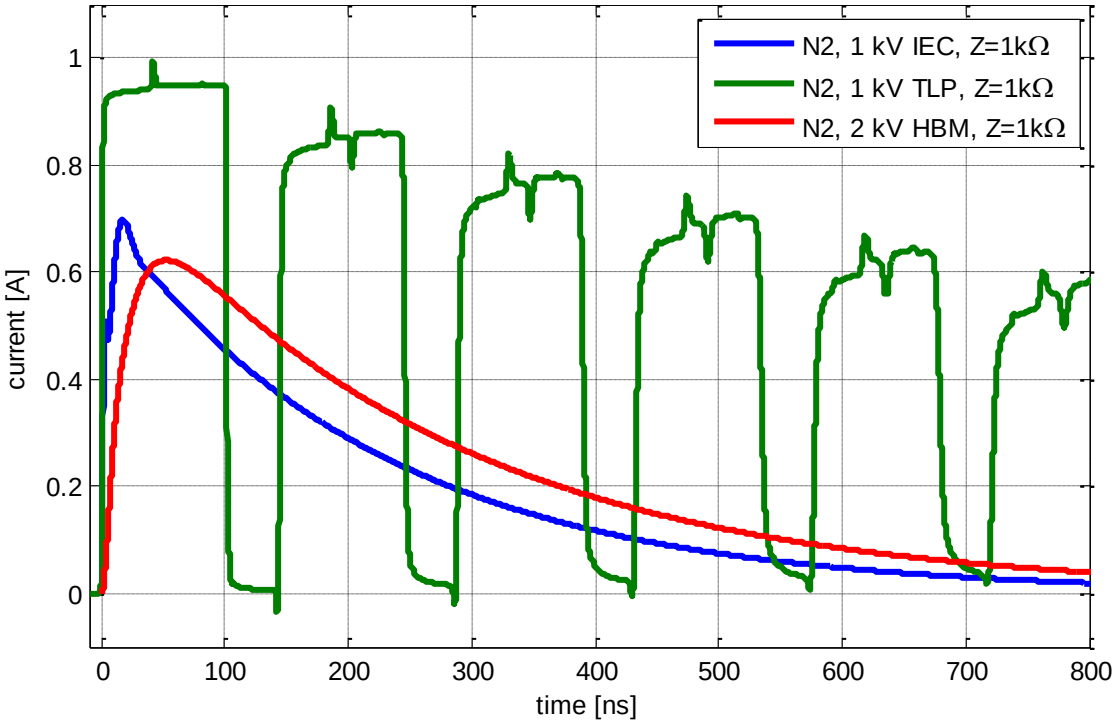

Figure 162: Simulated current at node 2 for Z = 1 kΩ

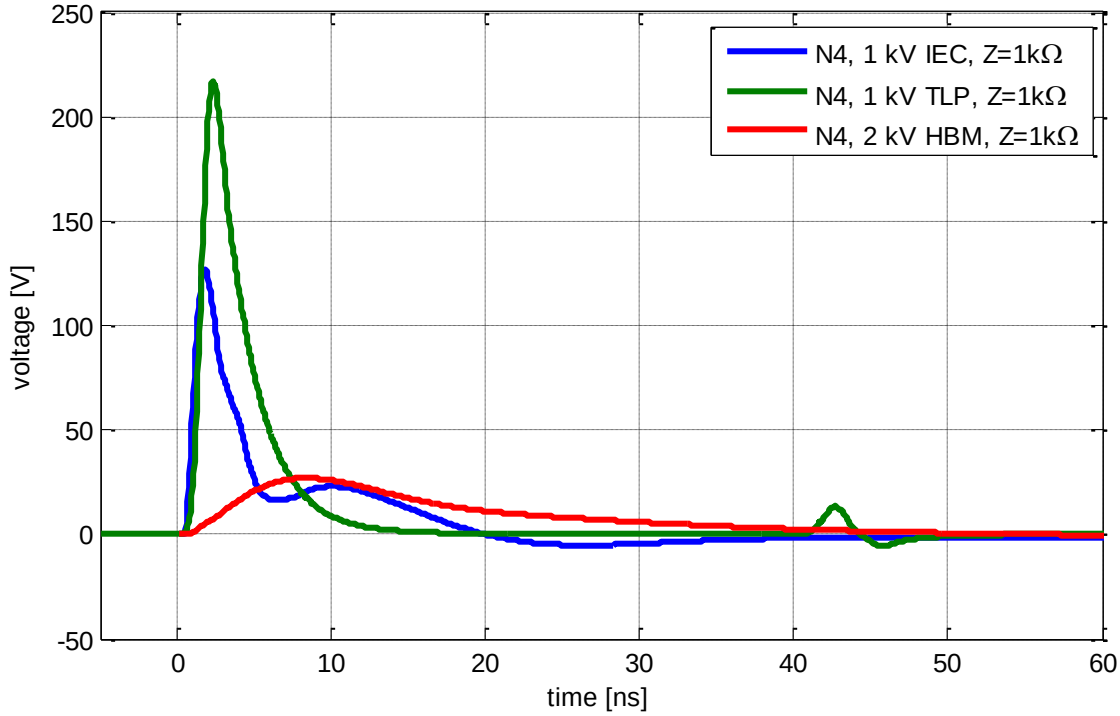

Figure 163: Simulated voltage at node 4 for Z = 1 kΩ

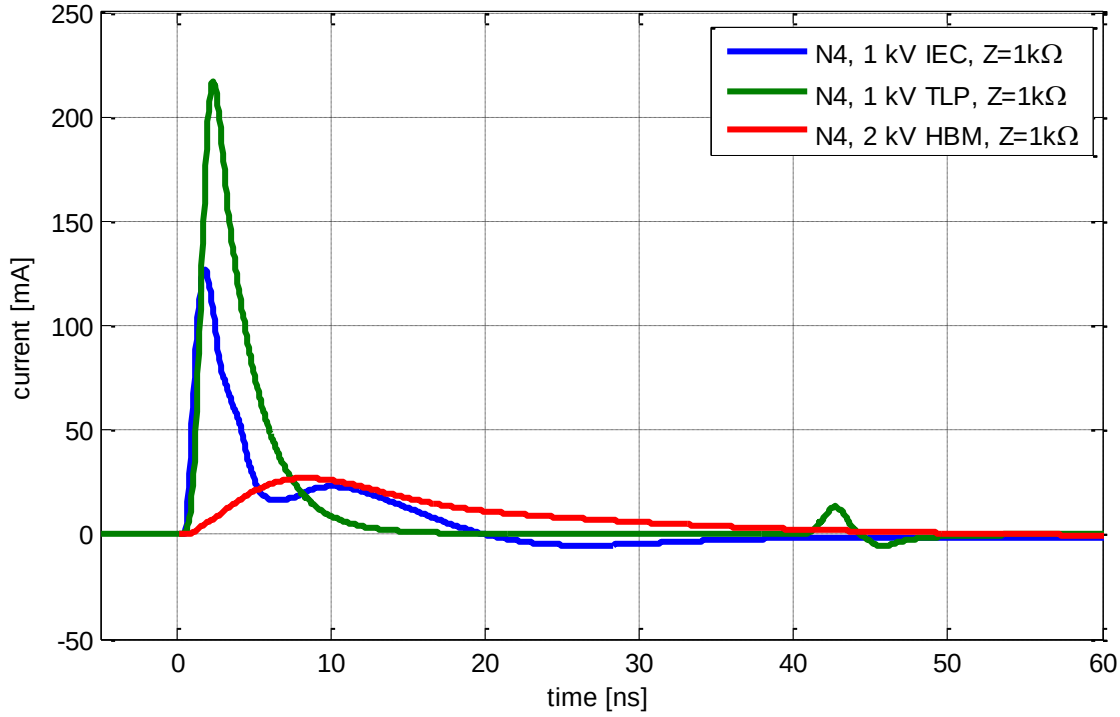

Figure 164: Simulated current at node 4 for Z = 1 kΩ

5.1.5 **Simulated waveforms for Z = 10 kΩ**

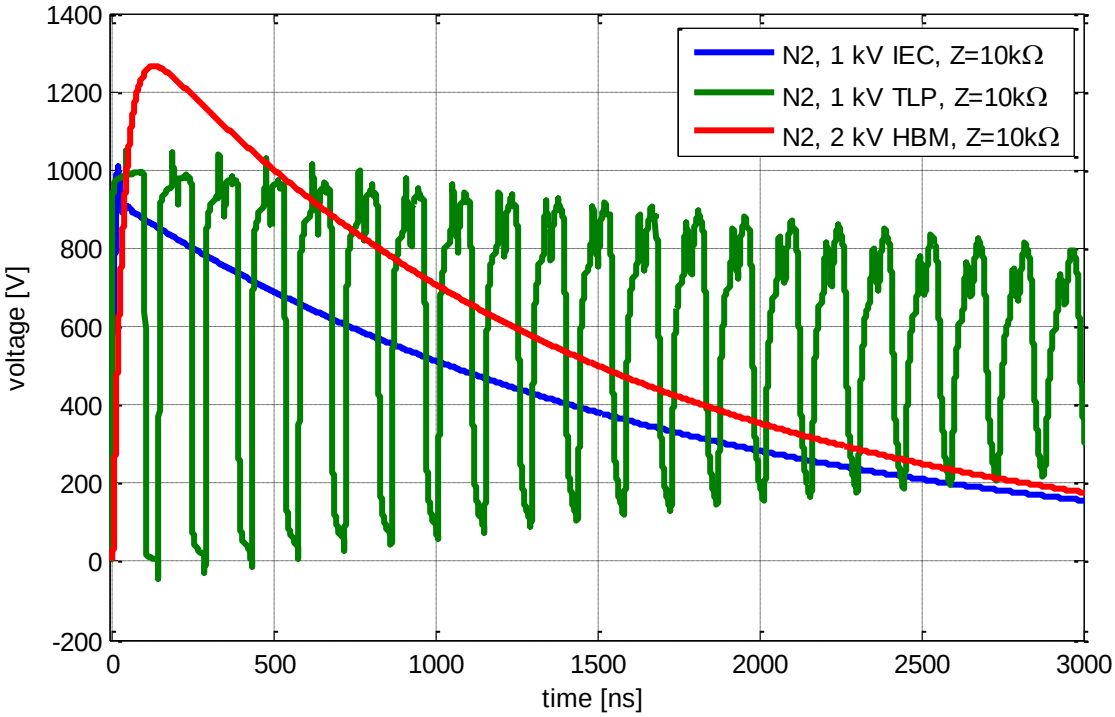

Figure 165: Simulated voltage at node 2 for Z = 10 kΩ

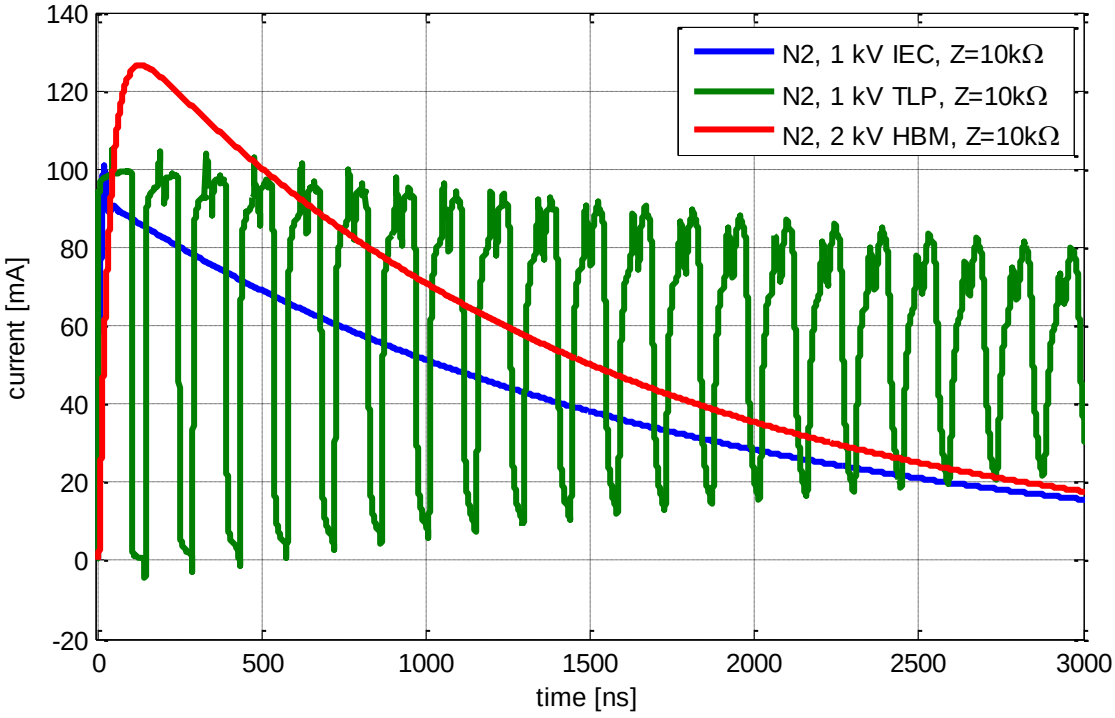

Figure 166: Simulated current at node 2 for Z = 10 kΩ

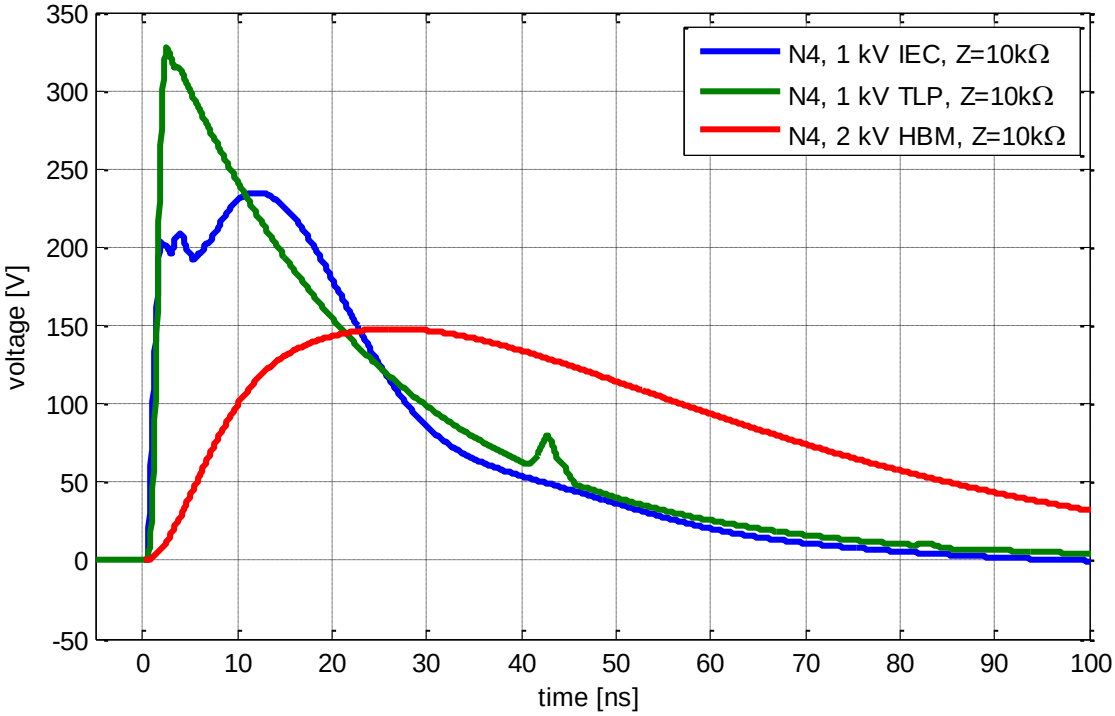

Figure 167: Simulated voltage at node 4 for Z = 10 kΩ

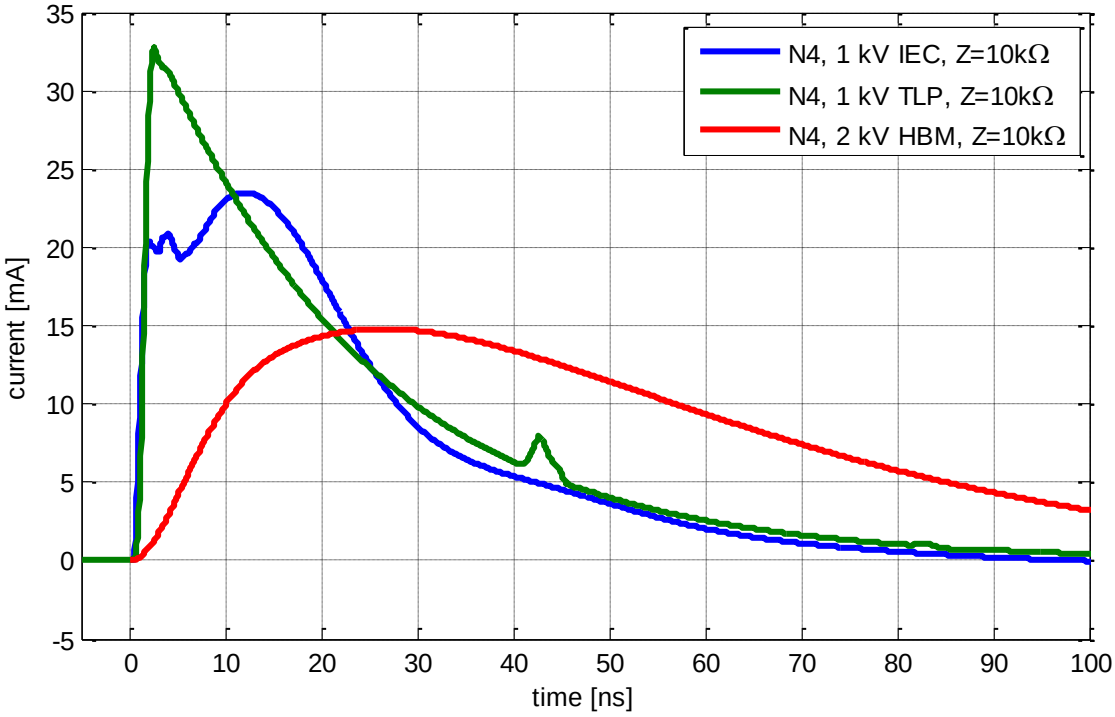

Figure 168: Simulated current at node 4 for Z = 10 kΩ

5.1.6 **Comparison of simulated maximum voltage amplitudes**

For all testing devices maximum amplitudes were simulated for the highest selected resistance Z (10 kΩ). In this case a factor 5 up to 6 was found between amplitudes simulated at the end of PCB trace 1 and PCB trace 2. If low impedance values are defined for Z, the factor 3 was found between the maximum simulated IEC voltages at node 2 and node 4. Although amplitudes are low in comparison to high impedance loads, coupling could be strong due to smaller rise times.

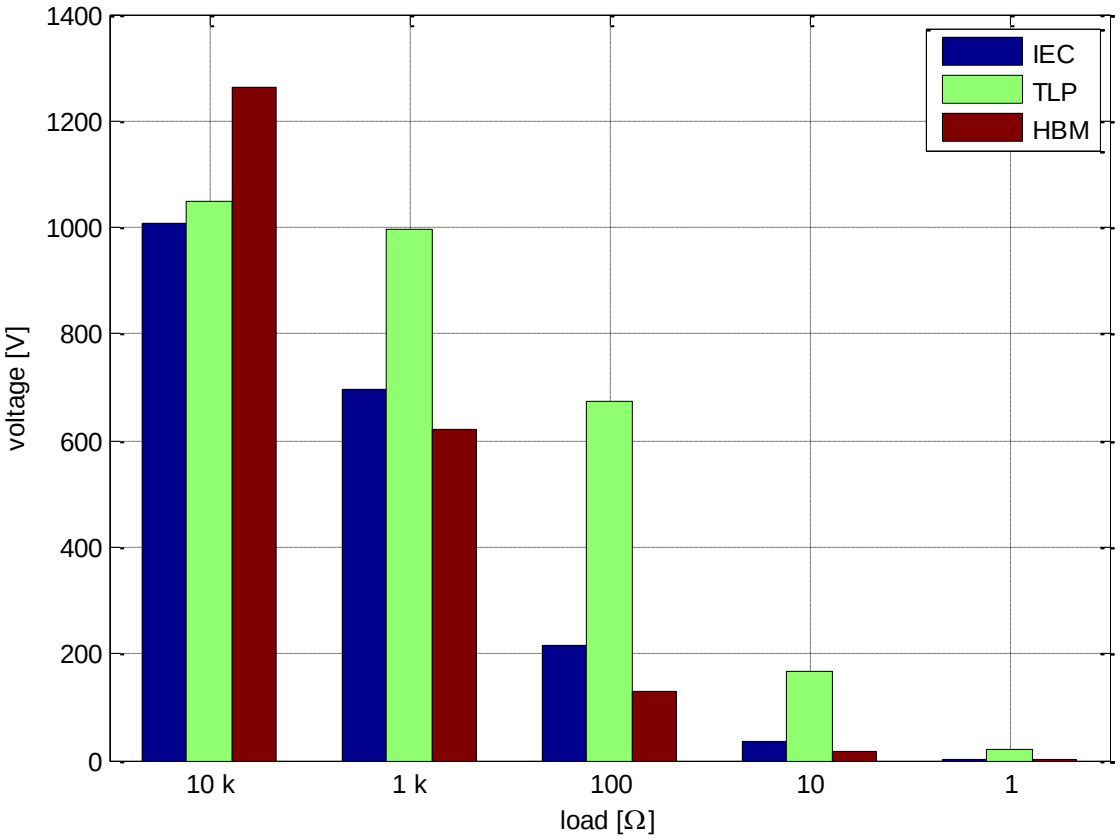

Figure 169: Comparison of simulated maximum voltage over different loads at node 2

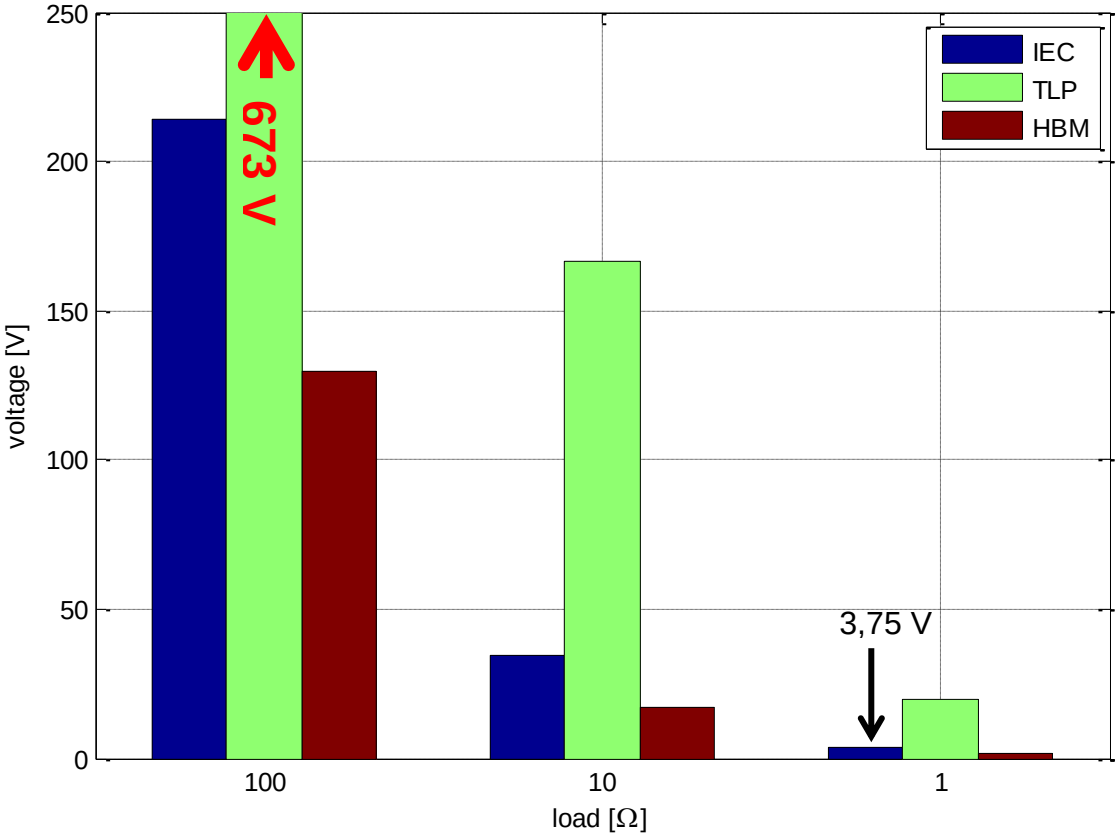

Figure 170: Comparison of simulated maximum voltage for small resistance at node 2

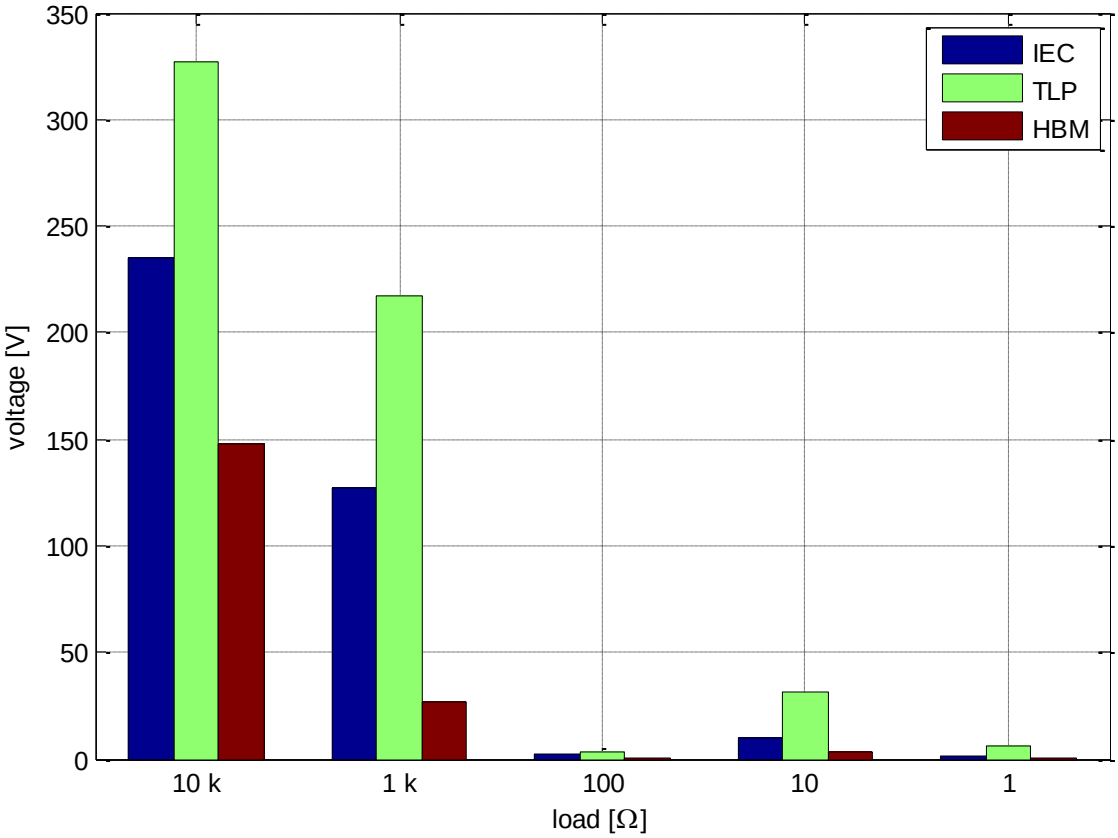

Figure 171: Comparison of simulated maximum voltage over different loads at node 4

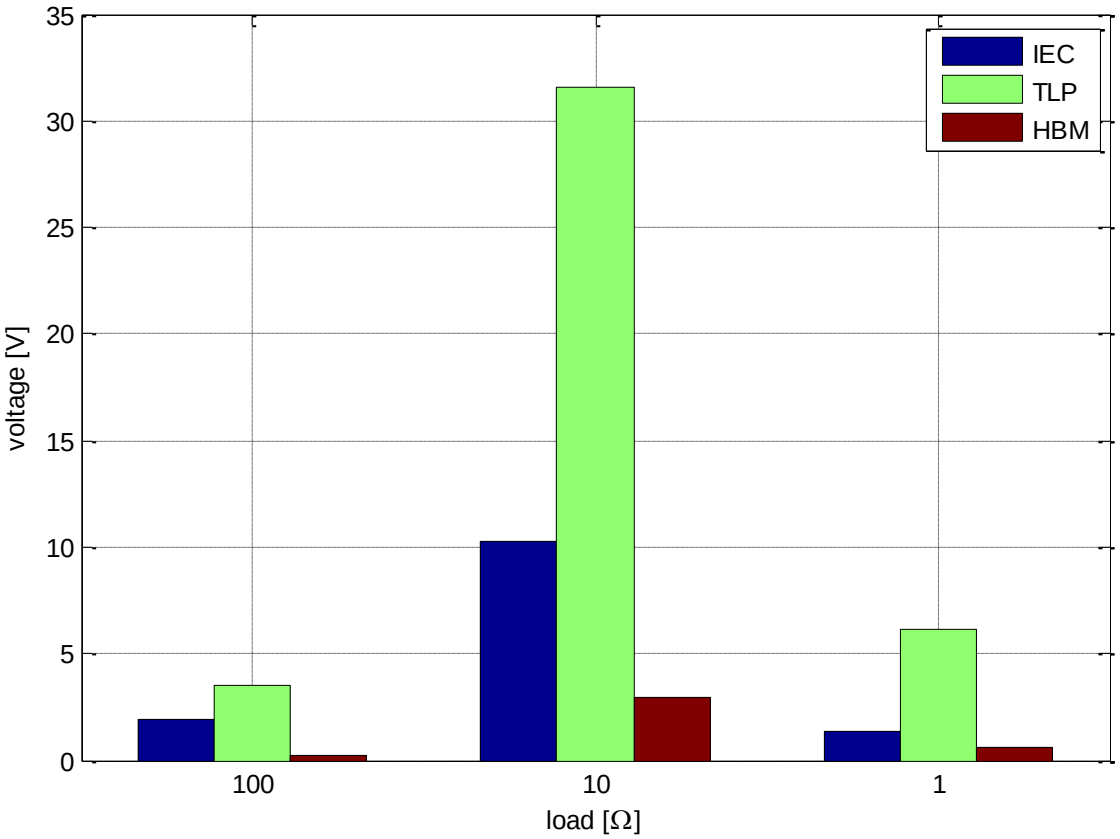

Figure 172: Comparison of simulated maximum voltage for small resistance at node 4

5.1.7 **Comparison of energy coupled by the different generators**

Since the IEC generator is defined as a standard testing device for automotive electronics on system level, the calculated energies are normalized to 75 µJ (reference value), which is the energy stored in 150 pF at 1 kV charge voltage ($W = \frac{1}{2} C V^2$). In Figure 173 and Figure 174 the voltage and current waveforms, where a charged IEC Generator with internal discharge resistor of 330 Ω is discharged via another 330 Ω resistor, are shown. The provided energies reach less than the half of the reference energy as shown in Figure 175. The provided energy is lower because of additional lossy circuit elements in the IEC model.

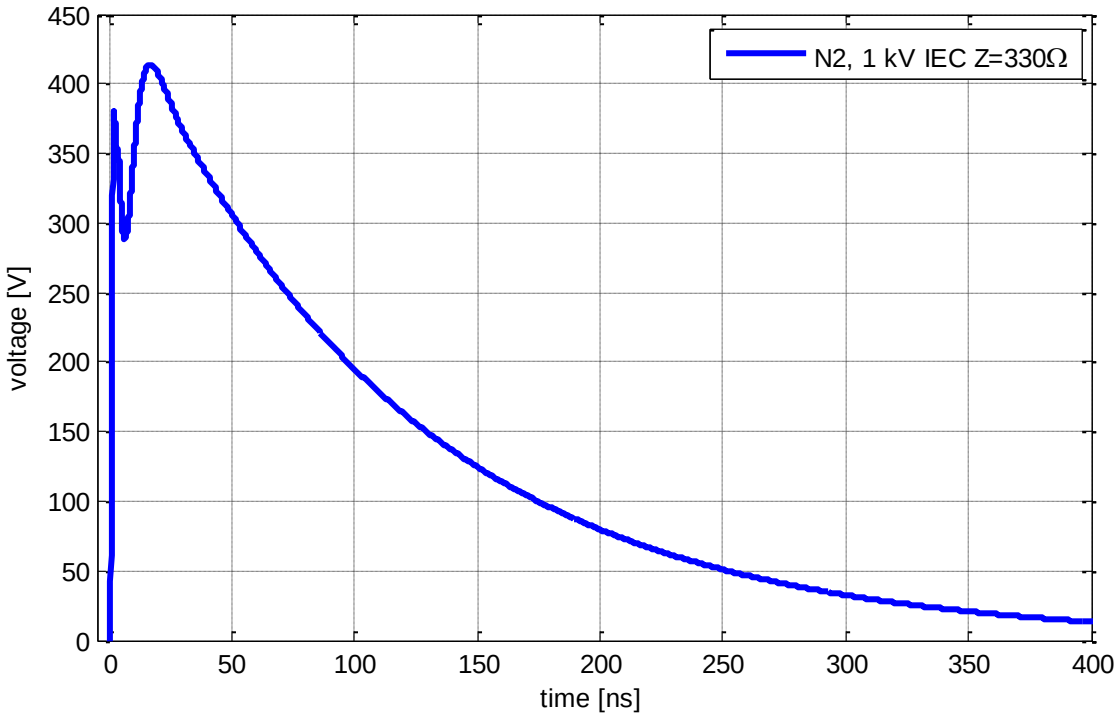

Figure 173: Simulated voltage for a 1 kV IEC generator discharge into 330 Ω

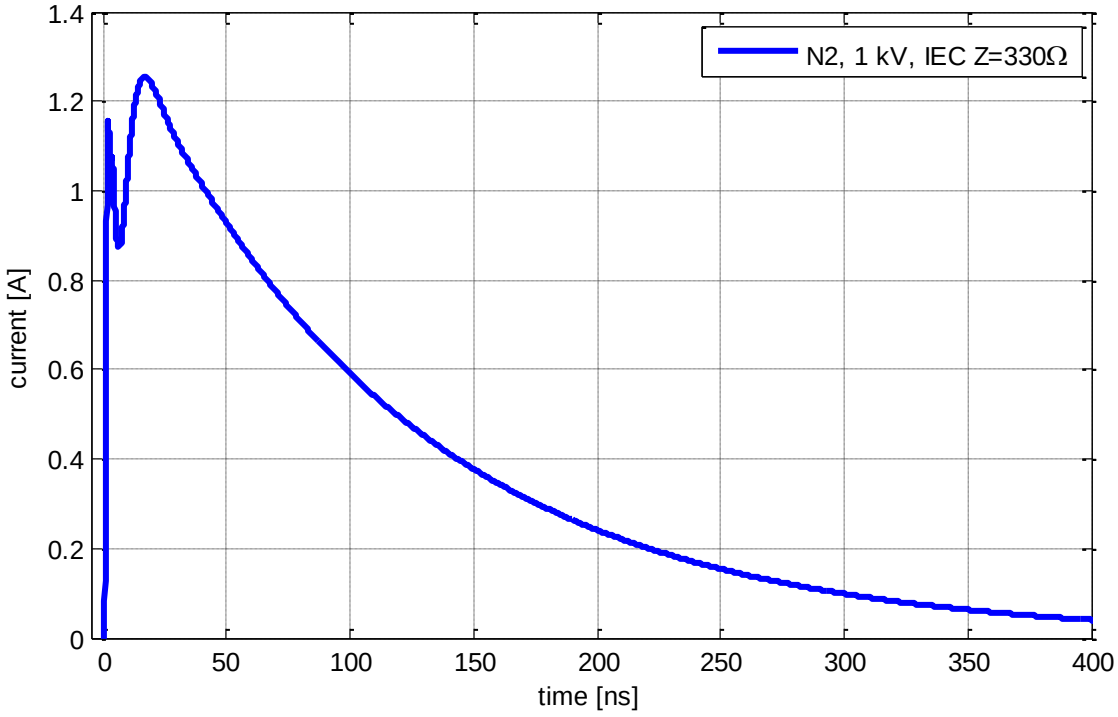

Figure 174: Simulated current for a 1 kV IEC generator discharge into 330 Ω

In case of the simulated TLP discharge many reflections due to mismatch of the transmission lines appear. For a comparison to IEC and HBM discharges the corresponding TLP energies are calculated up to the moment when the falling edge of the IEC pulse has decayed to 10 % of its maximum amplitude for a certain load. The calculated times are listed in Table 6.

Termination	Time for 90 % drop off falling edge
1 Ω	100 ns
10 Ω	150 ns
100 Ω	190 ns
1 kΩ	500 ns
10 kΩ	3500 ns

Table 26: IEC 10% decay times used for calculation of TLP energy

The simulated energies of each pulse generator are shown in Figure 175 to Figure 180. Amplitudes at both PCB trace ends are comparable. For IEC and HBM generator the amplitudes of coupled energies are of factor 1000 lower than the impressed energy on PCB trace 1. The highest voltage amplitudes are simulated if the load resistance is set to 10 kΩ except for the TLP generator. In this case the biggest differences related to the 1 kV IEC pulse energy were obtained for the 100 Ω termination because of a good power matching of the TLP impedance.

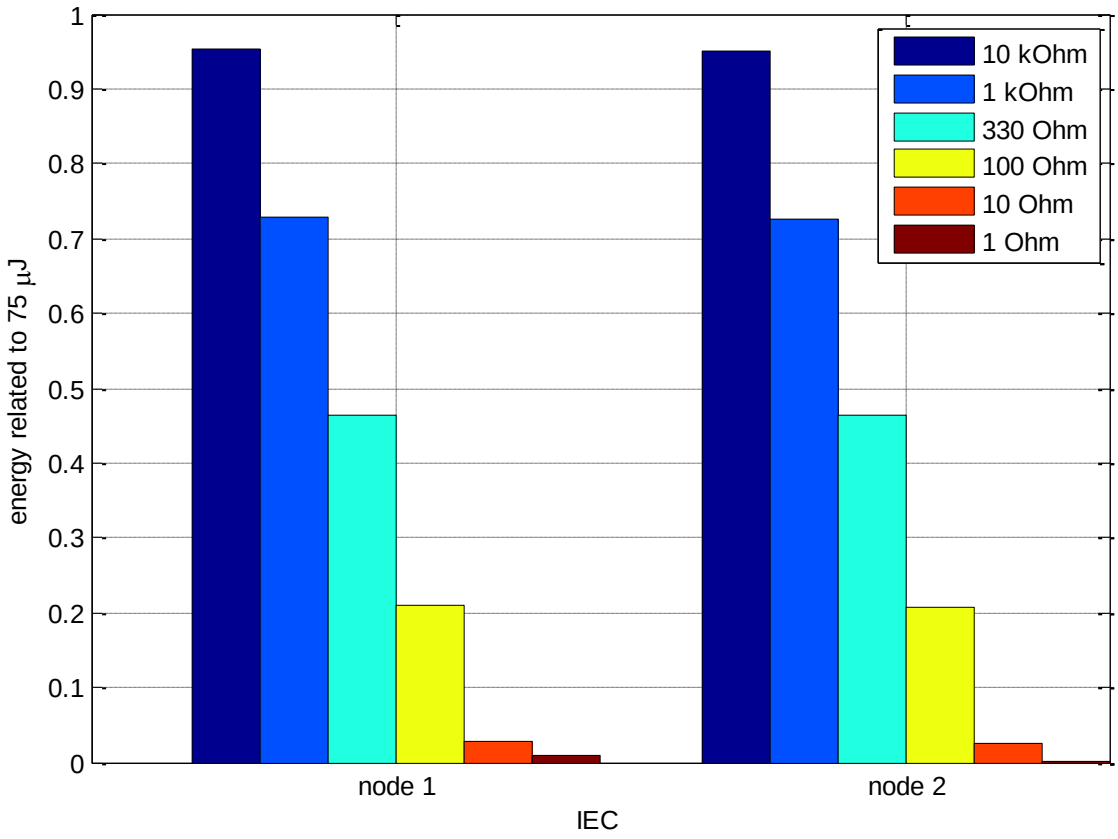

Figure 175: Comparison of simulated energies for an IEC generator

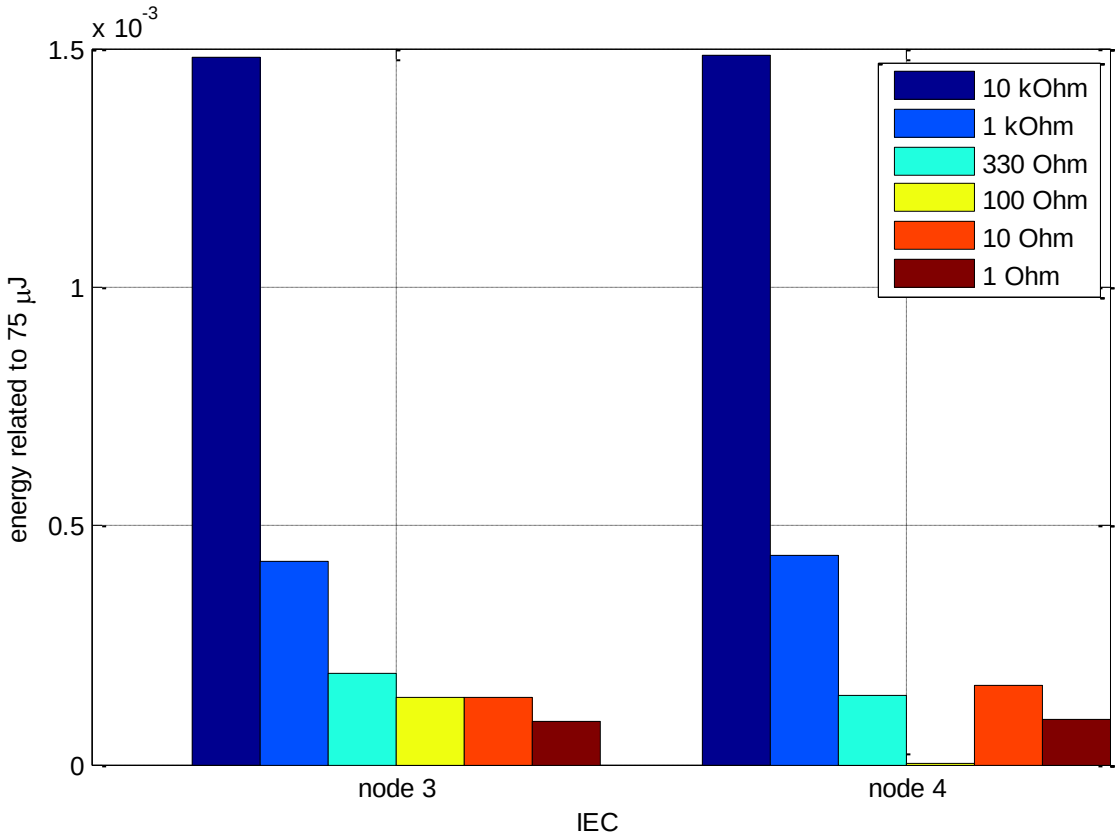

Figure 176: Comparison of simulated coupling energies for an IEC generator

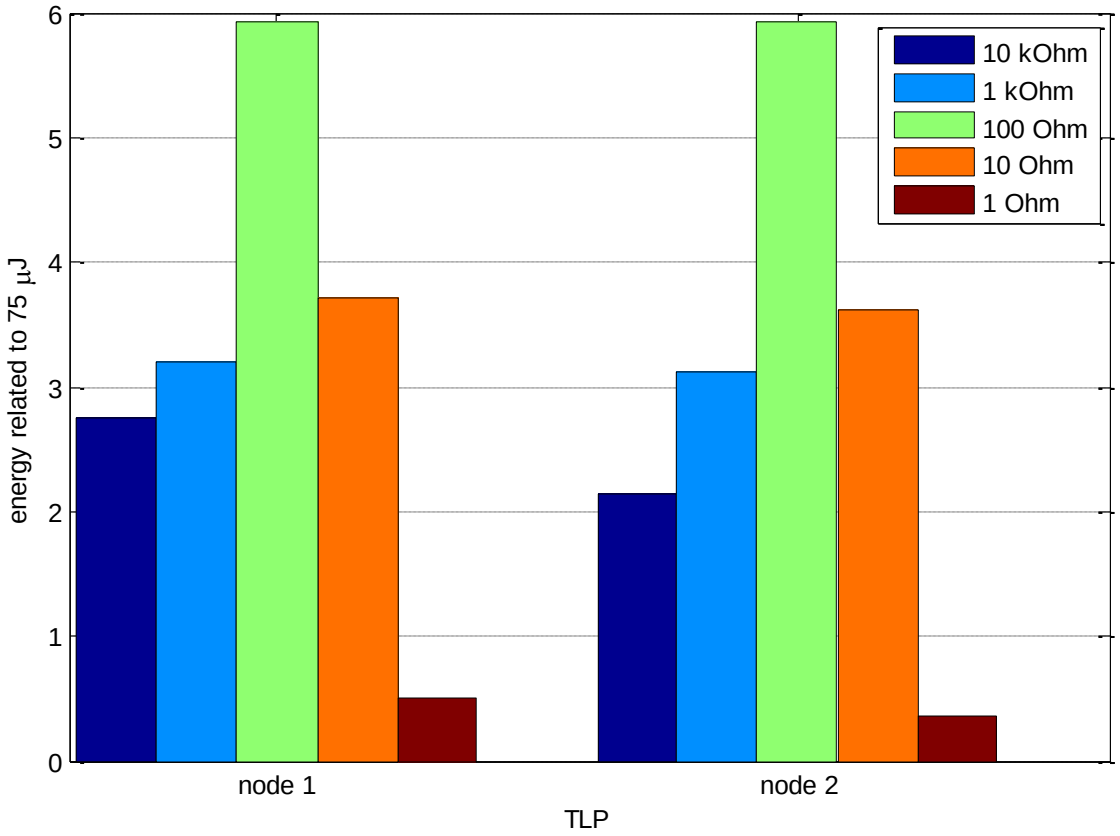

Figure 177: Comparison of simulated energies for a TLP discharge

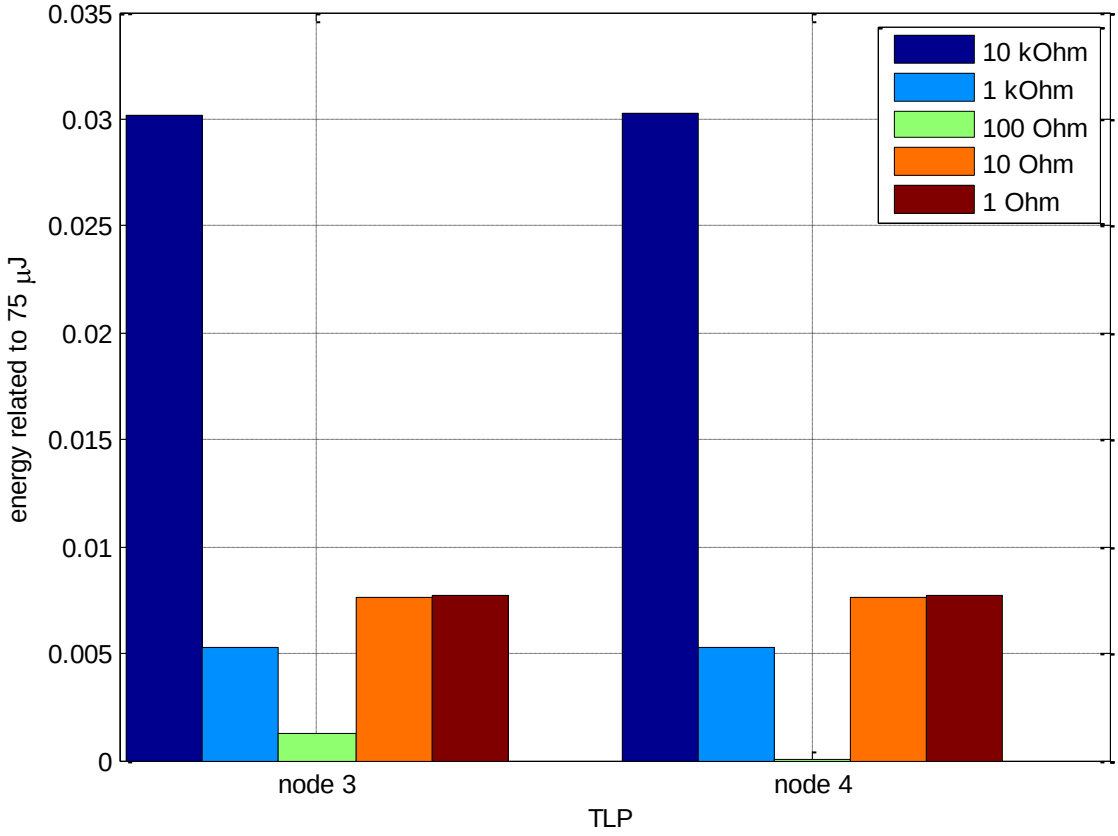

Figure 178: Comparison of simulated coupling energies for a TLP

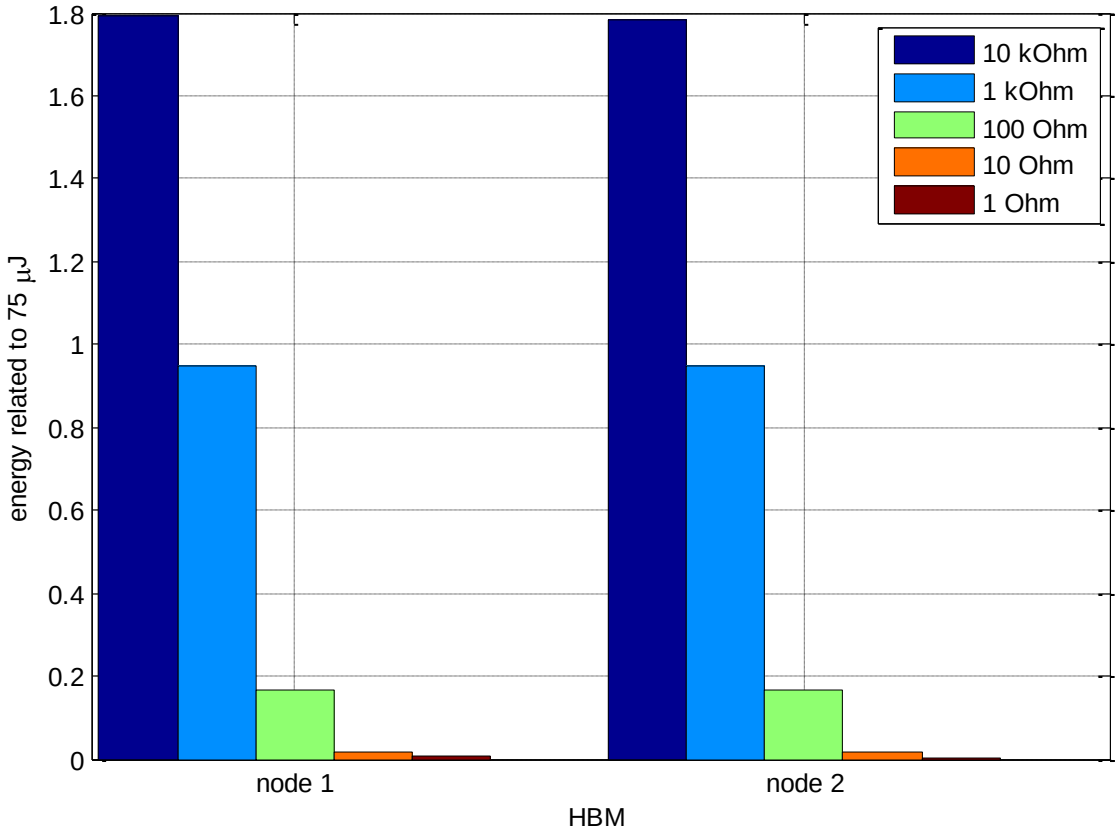

Figure 179: Comparison of simulated energies for an HBM generator

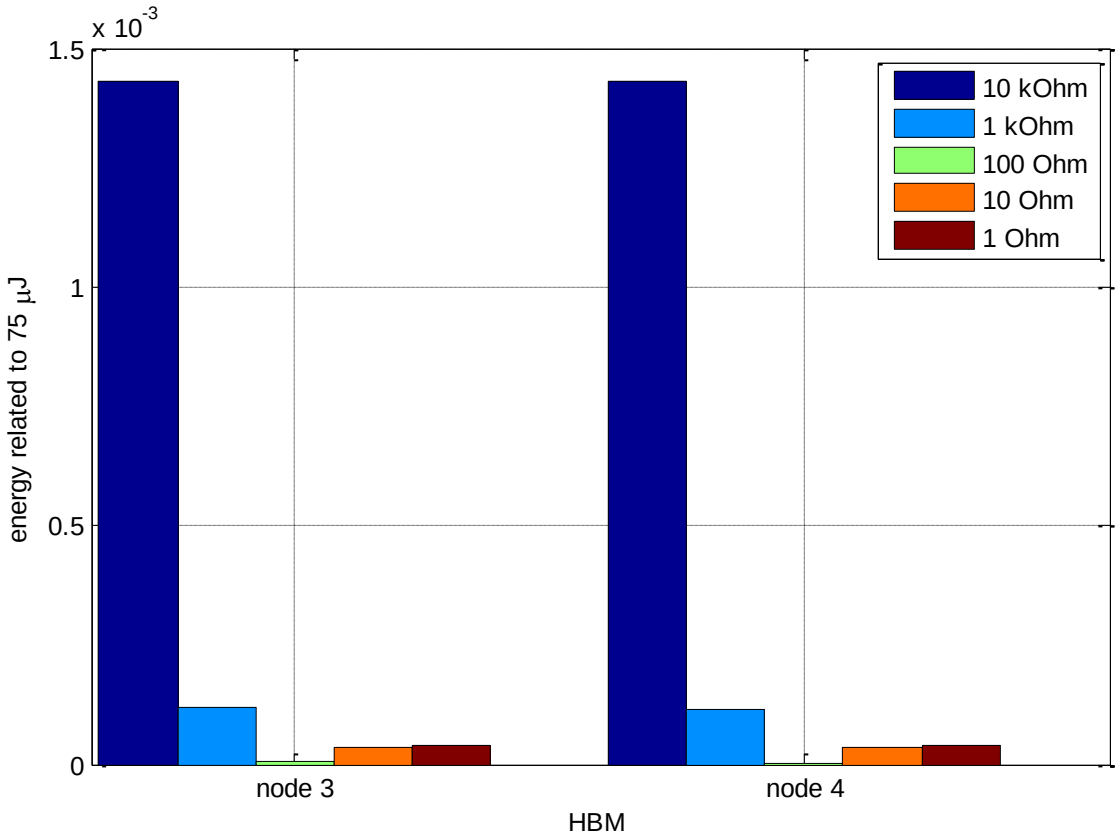

Figure 180: Comparison of simulated coupling energies for an HBM generator

The amount of coupled energy mainly depends on the voltage drop on transmission line 1. A high resistance Z leads to higher voltage over the load. The shortest rise times usually are obtained for shorted conductors. As only ohmic values for Z were chosen, the effect on rise times is low. In Figure 167 the highest coupled voltage amplitude was simulated for the IEC discharge.

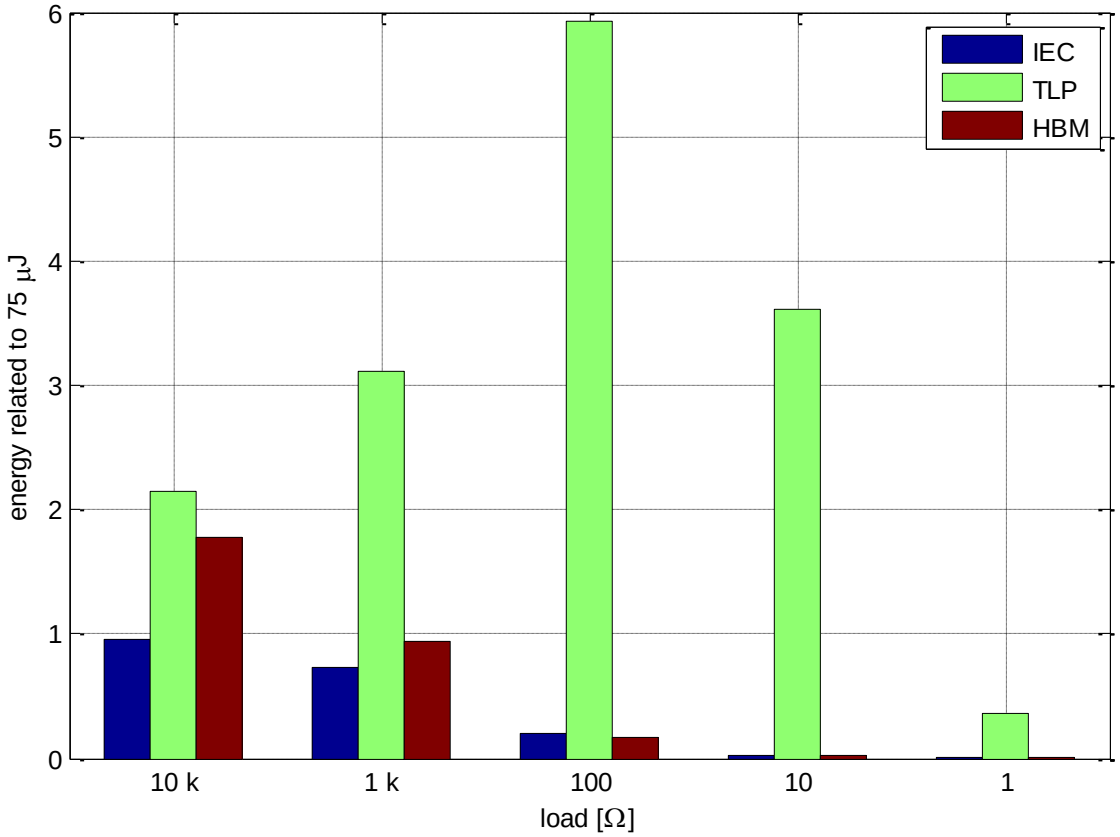

Figure 181: Comparison of simulated energies at node 2 for IEC, TLP and HBM generators

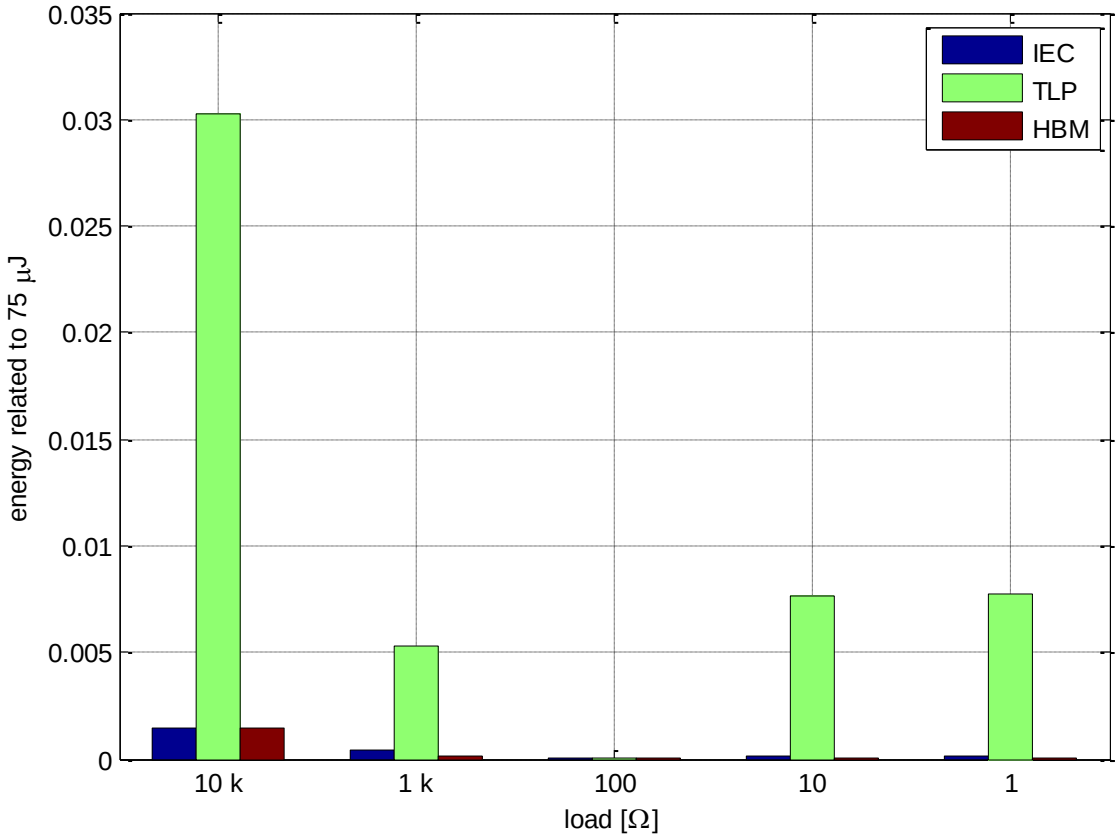

Figure 182: Comparison of simulated energies at node 4 for IEC, TLP and HBM generators

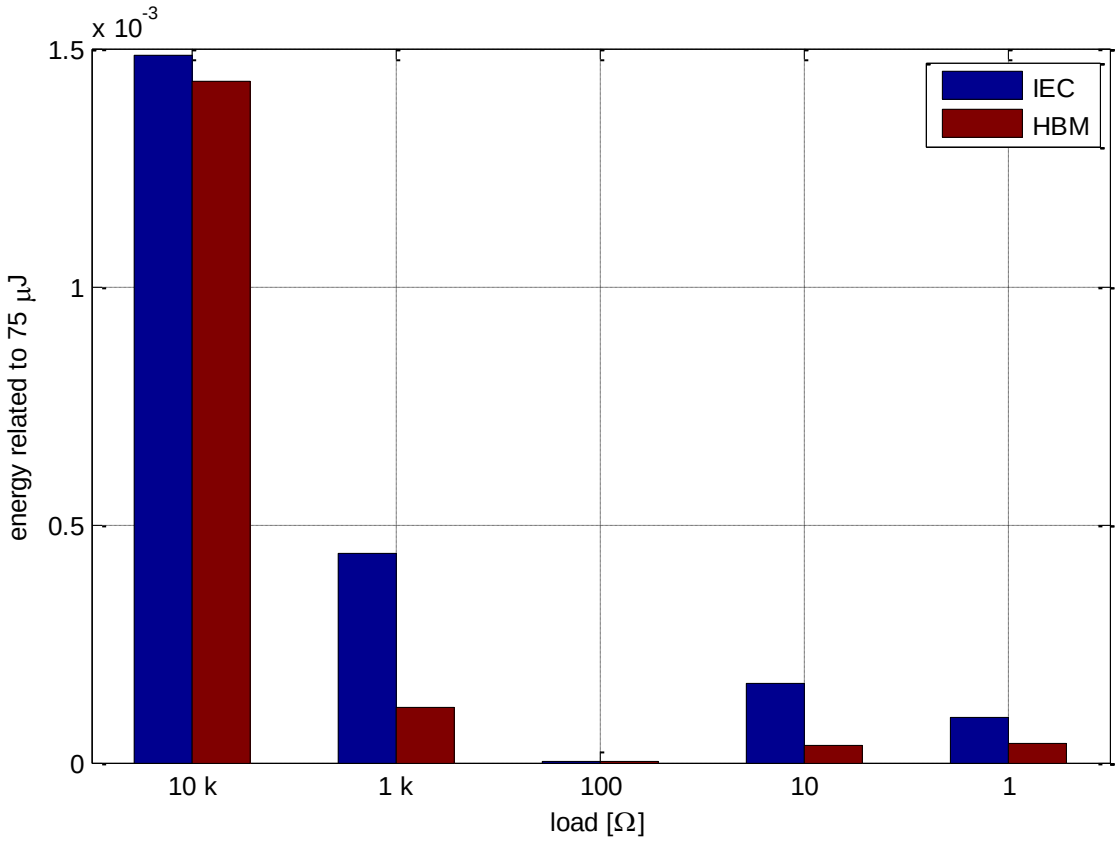

Figure 183: Comparison of simulated energies at node 4 for IEC and HBM generators

5.2 Impact of charging voltage on coupled signals

Current and voltage waveforms of IEC discharges with different charging voltages are simulated. In the simulation model the parameters of the conductor configuration of the cross-talk section on the demonstrator PCB are used. The simulation model was verified by measurement in frequency domain in section 4.1 and in time domain in section 4.2.

5.2.1 **PCB traces terminated with resistors**

The simulation setup with resistors as loads is shown in Figure 184. Each PCB trace is terminated with 1 kΩ and 50 Ω resistors. The IEC ESD generator model is connected to the circuit at node N1.

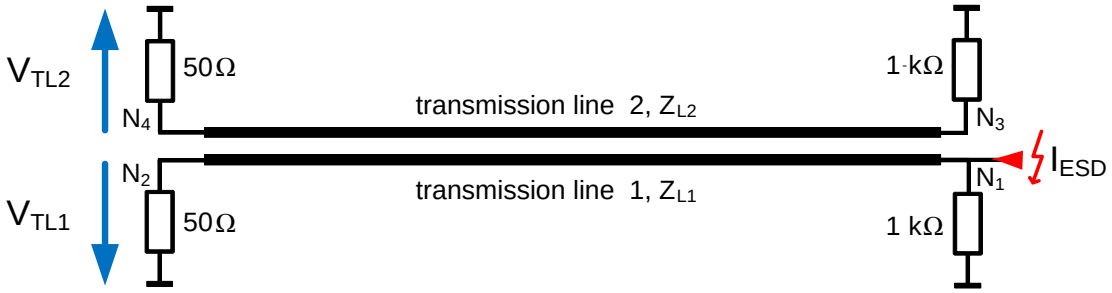

Figure 184: Topology with resistors as loads

In Figure 185 to Figure 188 the simulated voltage and current waveforms are given at nodes N2 and N4. Charging voltage level was set to 1 kV, 2 kV, 4 kV and 8 kV.

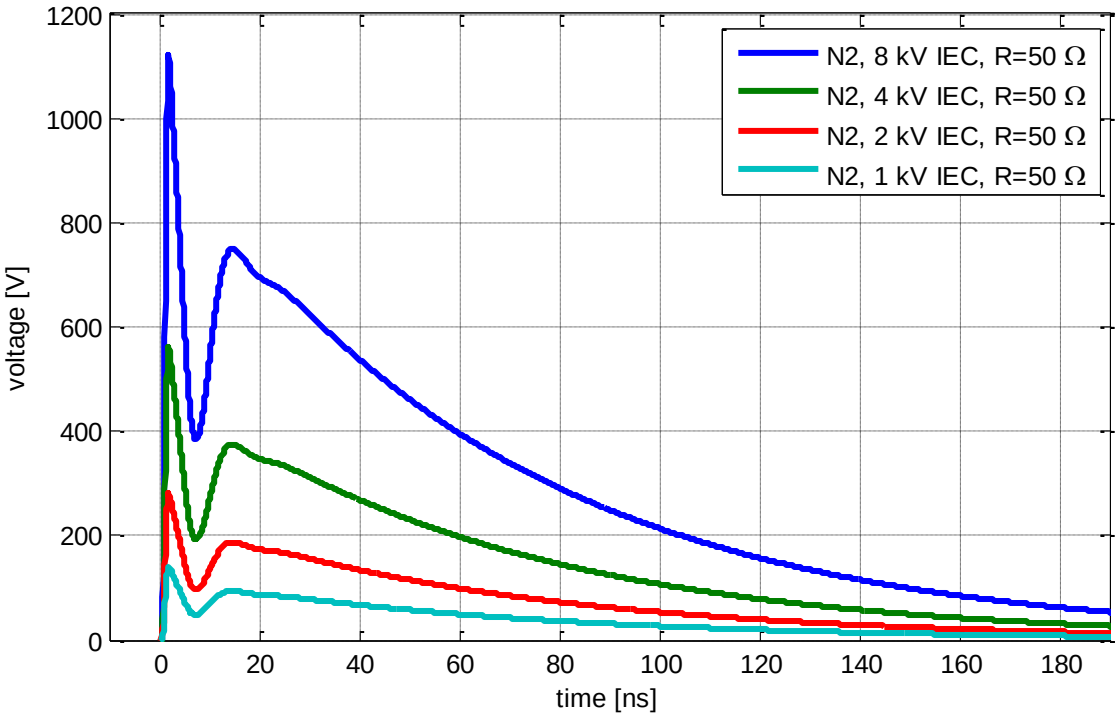

Figure 185: Voltage over 50 Ω at node N2

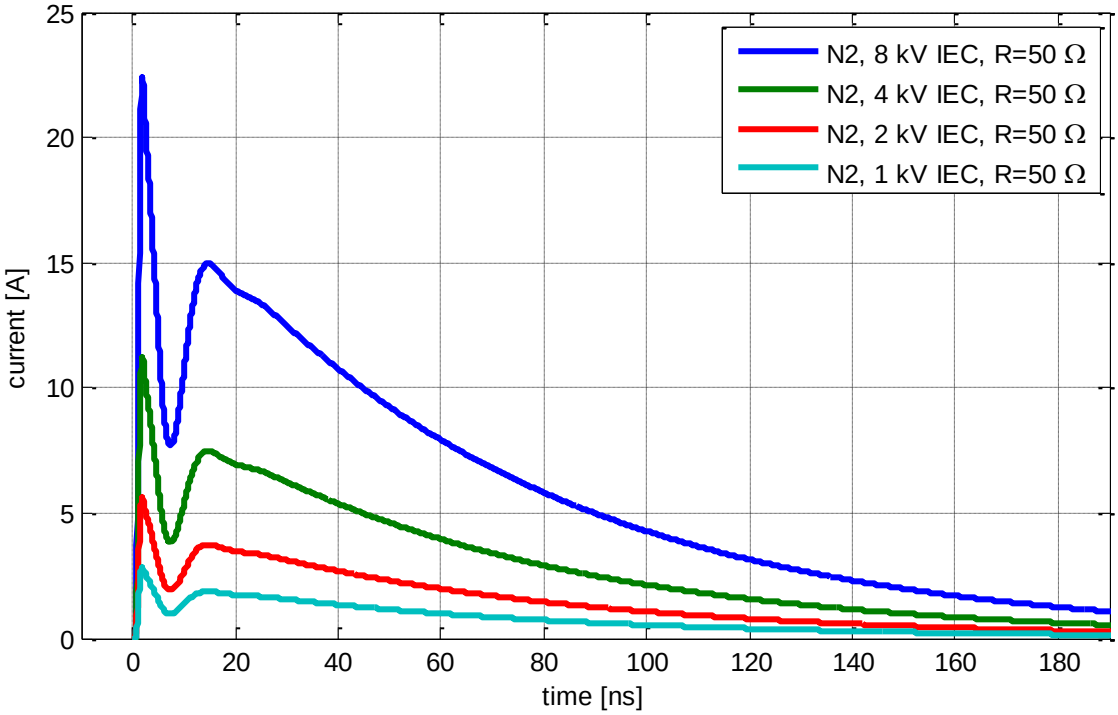

Figure 186: Current through node N2

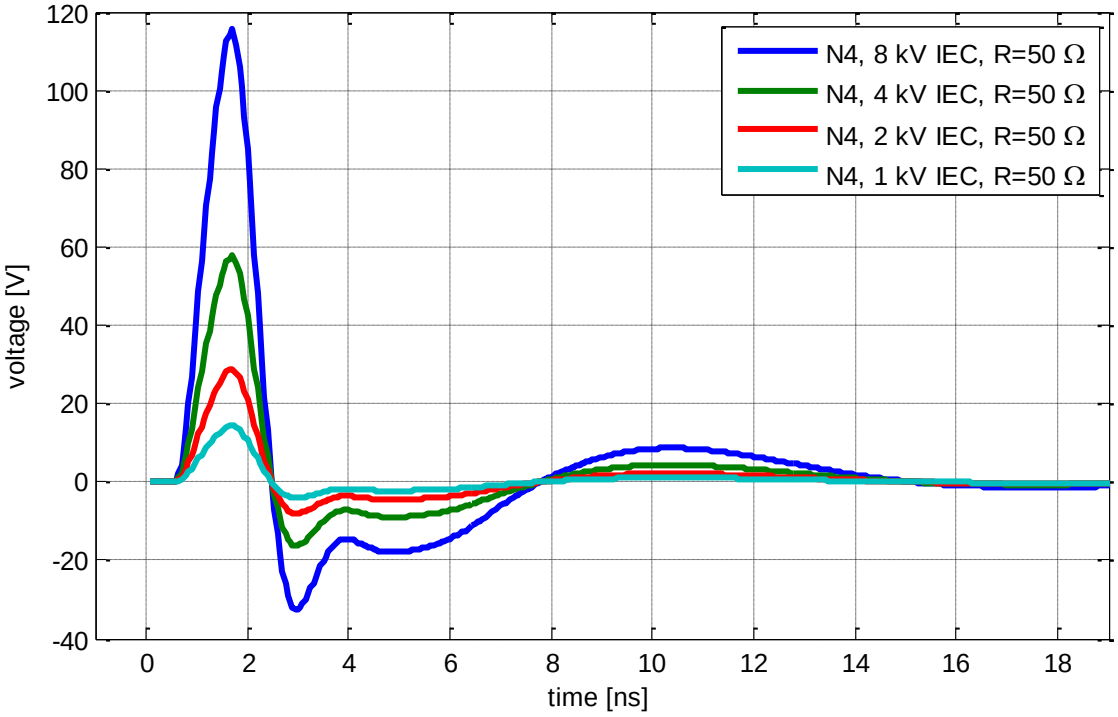

Figure 187: Voltage over 50 Ω at node N4

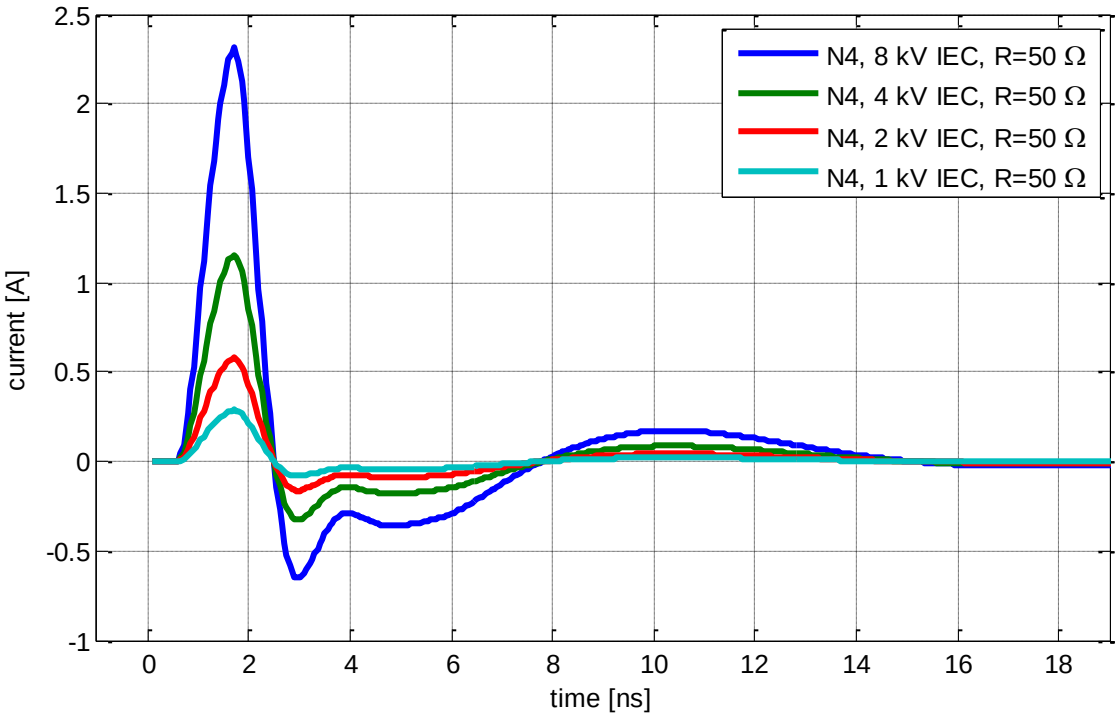

Figure 188: Current through node N4

In Table 27 and Table 28 the simulated maximum amplitudes and energies are compared for different charging voltages. The maximum simulated coupled energy is about 240 nJ. The factor ΔE expresses the energy for a charging voltage level related to the energy simulated for a 1 kV discharge. With linear resistive loads the ΔE factor is quadratic to the factor of charging voltage.

V_{charge} [kV]	V_{max} [V]	I_{max} [A]	E [µJ]	$E/E_{1\ kV}$
1	139,97	2,80	8,24	1
2	279,93	5,60	32,96	4
4	559,87	11,20	131,84	16
8	1119,7	22,40	527,35	64

Table 27: Simulated quantities at node N2

V_{charge} [kV]	V_{max} [V]	I_{max} [A]	E [nJ]	$E/E_{1\ kV}$
1	14,47	0,29	3,73	1
2	28,94	0,58	14,92	4
4	57,87	1,16	59,67	16
8	115,75	2,32	238,68	64

Table 28: Simulated quantities at node N4

5.2.2 **Transmission lines terminated with IC IV-characteristics**

More interesting than the linear case are nonlinear terminations of the investigated ICs. In Figure 189 the 50 Ω resistors at nodes N2 and N4 are replaced by the CANH model on PCB trace 1 and by the µC DATA model on PCB trace 2. The voltage and current amplitudes are simulated at the IC pins.

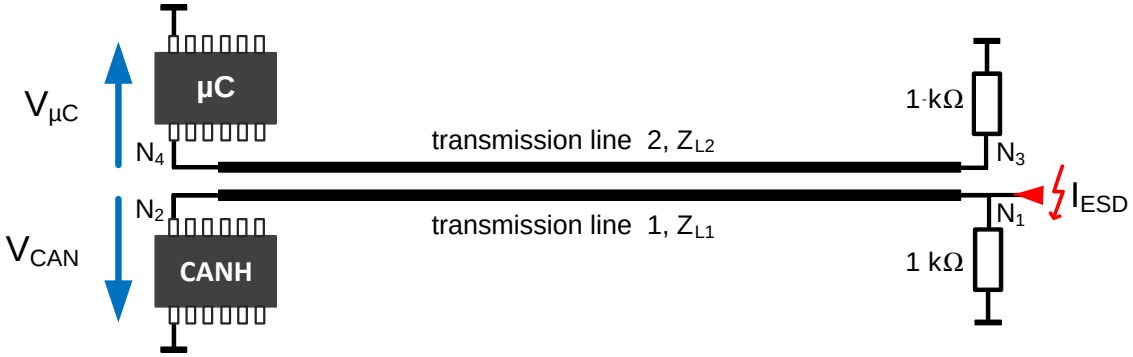

Figure 189: Topology with ICs as loads

Because of the IV characteristic of the IC models the voltage amplitudes at node N2 are attenuated in comparison to the configuration with resistors. The waveforms on transmission line 1 are shown in Figure 190 and Figure 191.

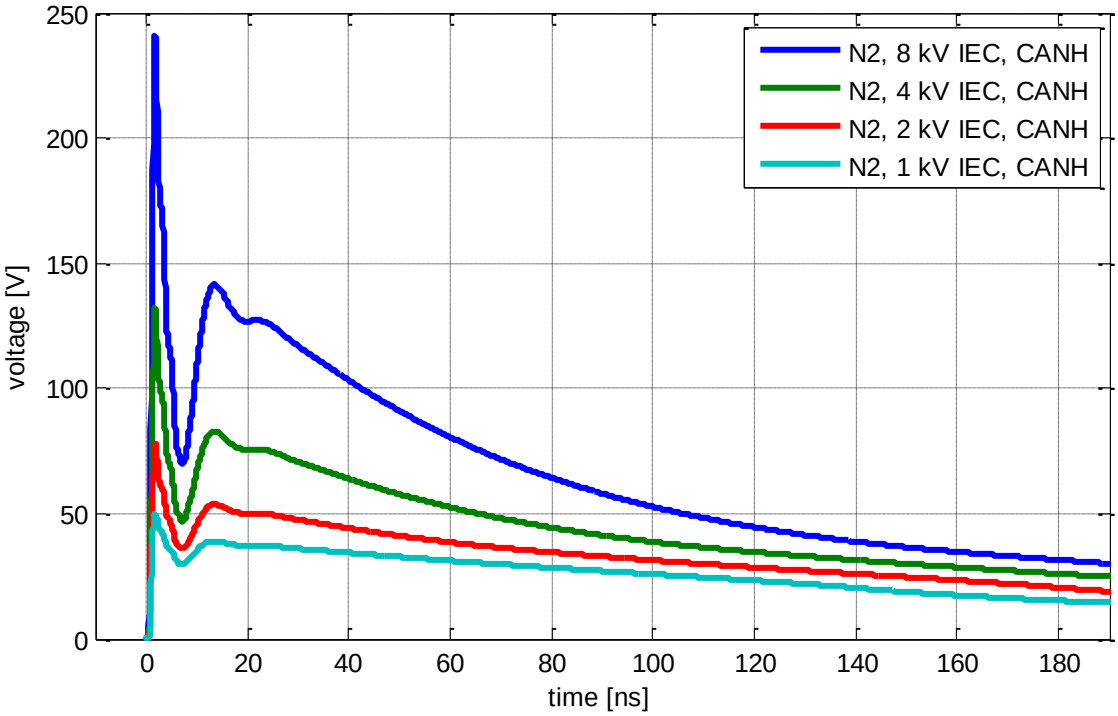

Figure 190: Simulated voltage at CANH-pin at node N2

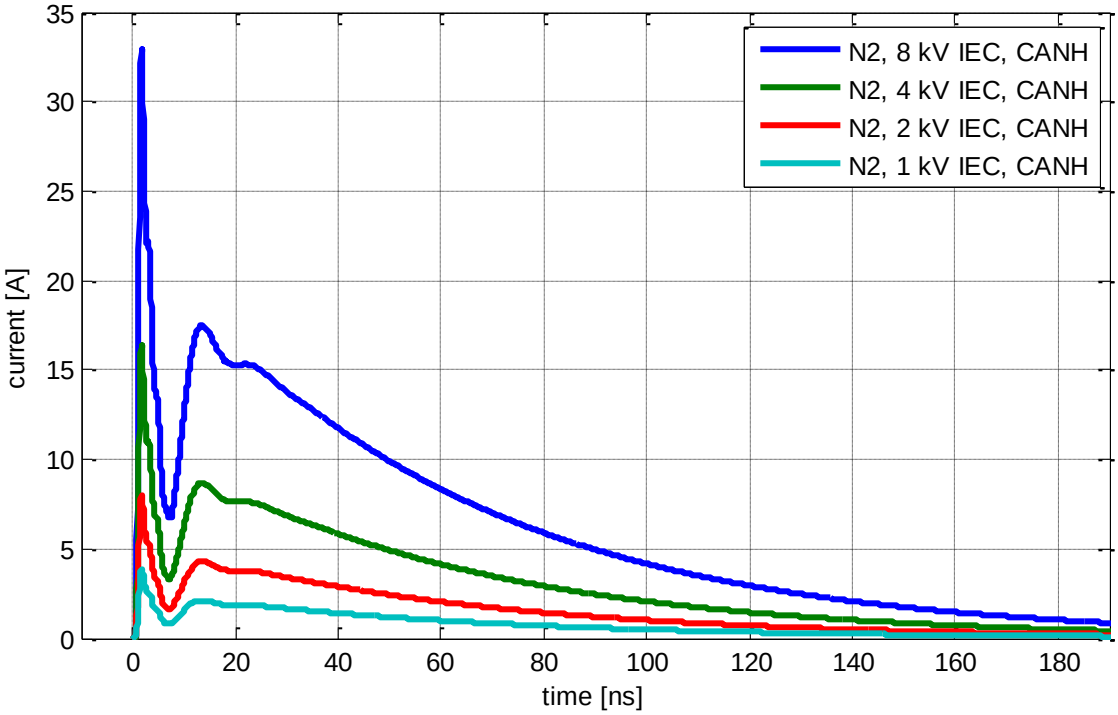

Figure 191: Simulated current through CANH pin at node N2

Clamping effects are observed for the waveform on transmission line 2 because of the IC IV characteristic. The peak voltage is limited for different charging voltage levels to about 3 A. Current amplitudes are decreased to less than 10 % in comparison to the topology with resistors. In Figure 192 and Figure 193 the voltage and current waveforms dominated by strong ringing are shown.

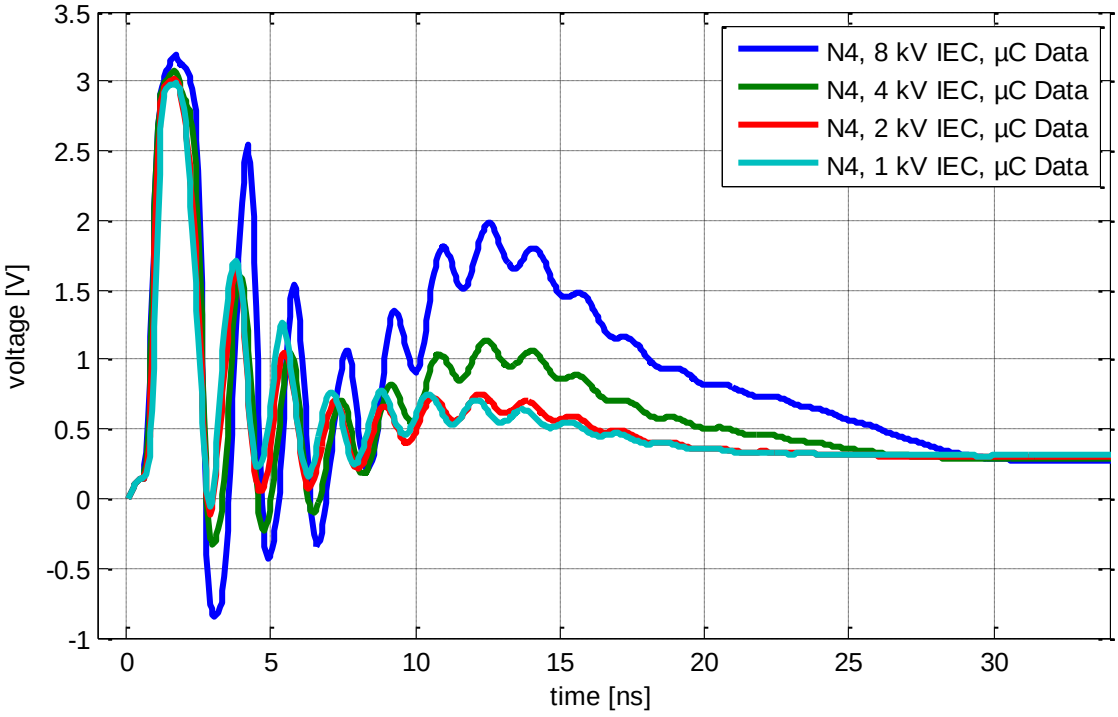

Figure 192: Simulated voltage at µC Data pin at node N4

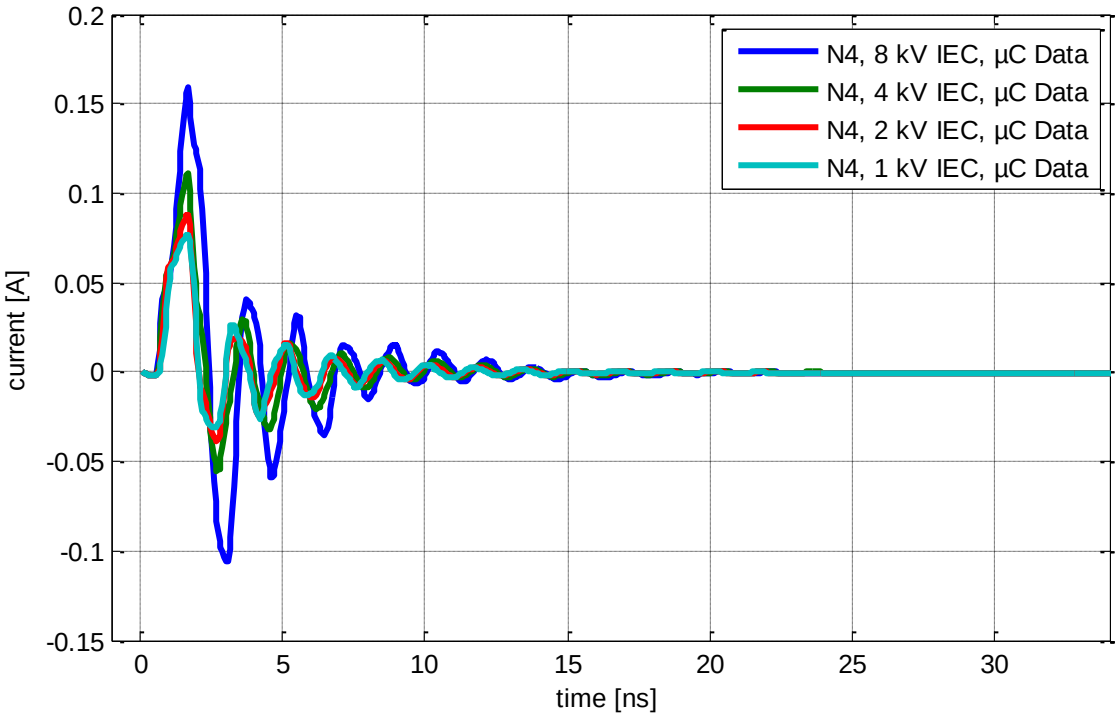

Figure 193: Simulated current through µC Data pin at node N4

The peak amplitudes and energies simulated at the CANH pin and at the DATA pin are compared in Table 29 and Table 30. The factors ΔE related to the energy of a 1 kV discharge are lower than for the setup with resistors. A factor 25 is obtained between the simulated energy for 8 kV IEC discharge at node N2 and 1 kV discharge compared to factor 64 with resistors. Factors ΔE simulated at the µC pin are even lower. The energy of the 8 kV discharge increases only about 2,5 times compared to 1 kV charging voltage.

V_{charge} [kV]	V_{max} [V]	I_{max} [A]	E [µJ]	$E/E_{1\ kV}$
1	50,24	3,86	4,67	1
2	77,52	8,03	12,42	2,66
4	132,01	16,36	35,99	7,71
8	240,90	32,96	115,51	24,73

Table 29: Simulated quantities at CANH-pin at node 2

V_{charge} [kV]	V_{max} [V]	I_{max} [A]	E [nJ]	$E/E_{1\ kV}$	Energy Coupling Factor (E_{N2}/E_{N4})
1	2,98	0,08	0,28	1	**16679**
2	3,02	0,09	0,29	1,06	**42828**
4	3,08	0,11	0,37	1,34	**97270**
8	3,18	0,16	0,68	2,46	**169870**

Table 30: Simulated quantities at µC Data pin at node 4

5.3 Effect of ESD protection elements on coupling signals

Similar to IC inputs, the electrical behavior of ESD protection elements such as varistors or diodes can be characterized by measurement of the IV characteristic. In this section the impact of the IEC charging voltage and protection elements is investigated for the parallel trace configuration.

5.3.1 50 Ω termination with protection element on PCB trace 2

Both transmission lines are terminated with 1 kΩ and 50 Ω resistors. An ESD protection element is connected parallel to the 1 kΩ resistor at transmission line 2. The setup is shown in Figure 105.

Simulated coupled voltage and current waveforms at the 50 Ω resistor at transmission line 2 are presented in Figure 194 and Figure 195 for 1 kV charging voltage and in Figure 196 and Figure 197 for 8 kV charging voltage. The reference curve with characteristic positive voltage and current peak was simulated without ESD protection element. If the protection device is connected in the simulation, higher amplitudes with negative prefix are obtained. The results can be referred to the capacitance of the protection elements. The capacitance of the TVS diode model was specified with 3 pF. Peak amplitude of about -17 V is simulated for 1 kV charging voltage. By connecting 10 nF a peak of about -26 V is obtained.

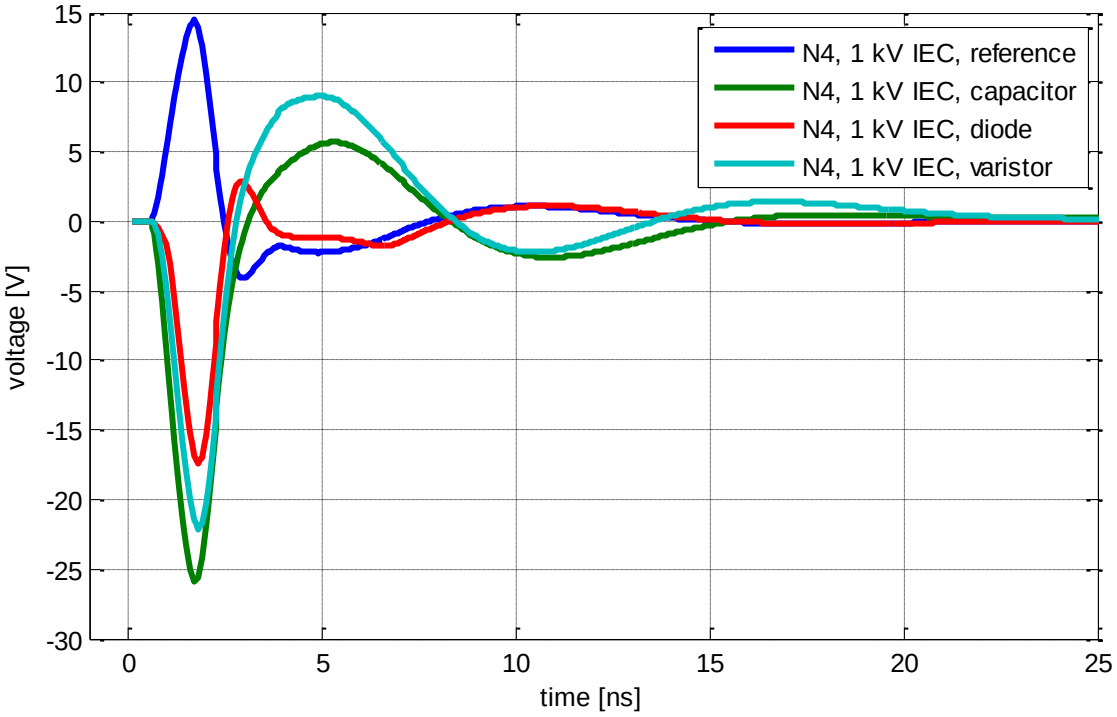

Figure 194: Simulated voltage on TL 2 for 1 kV IEC generator discharge on TL1

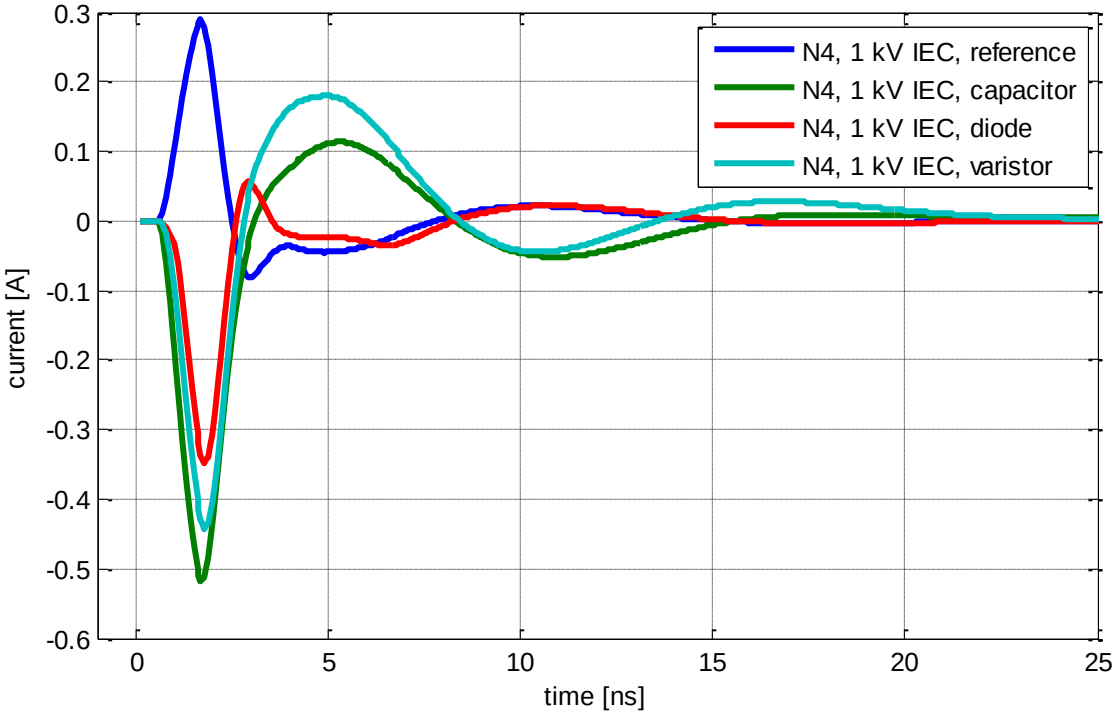

Figure 195: Simulated current on TL 2 for 1 kV IEC generator discharge on TL1

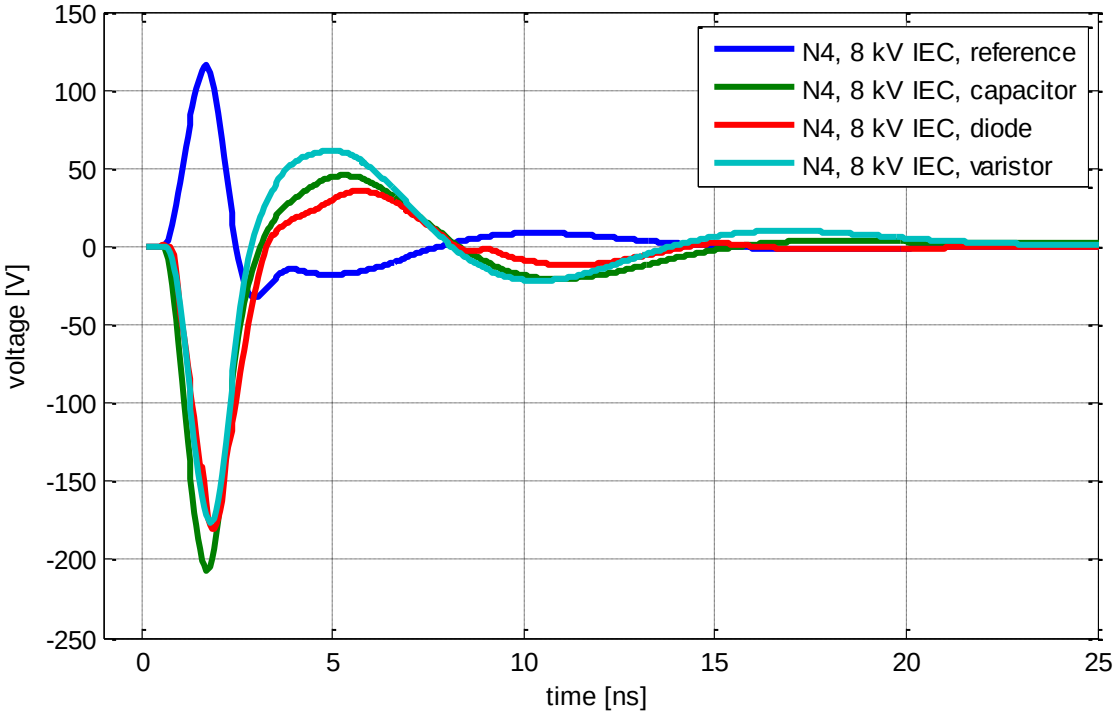

Figure 196: Simulated voltage on TL 2 for 8 kV IEC generator discharge on TL1

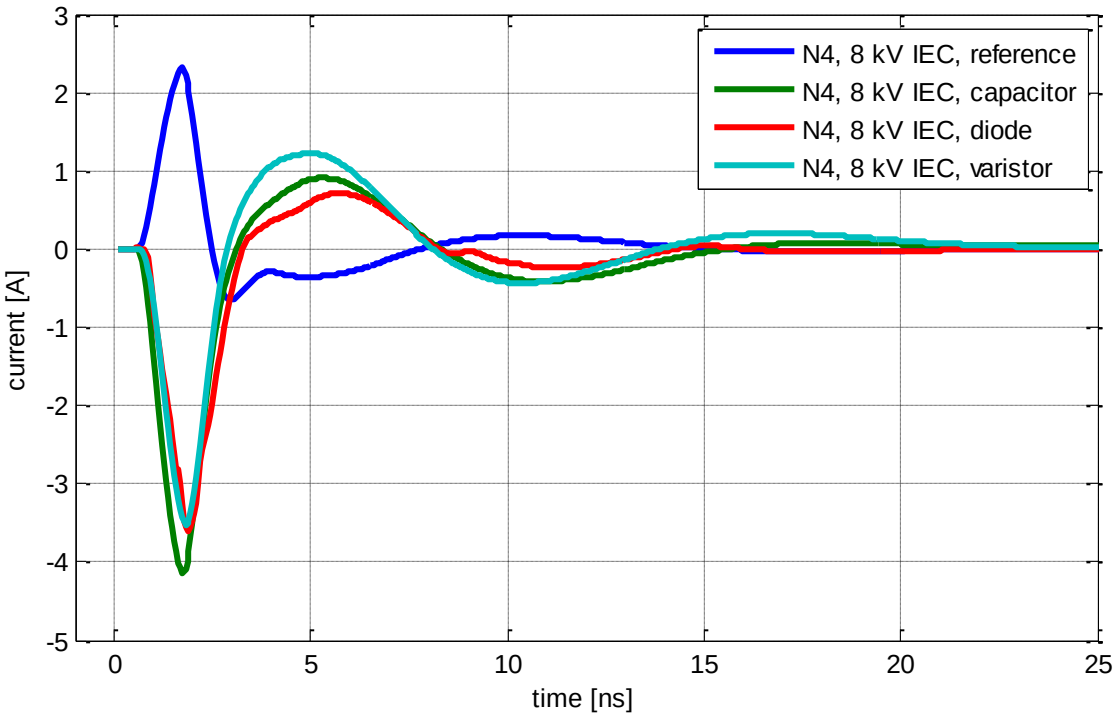

Figure 197: Simulated current on TL 2 for 8 kV IEC generator discharge on TL1

All simulated quantities for different levels of charging voltage are given in Table 31 for PCB trace 1 and in Table 32 for PCB trace 2. Because no device with non-linear IV characteristic is connected to PCB trace 1 the simulated amplitudes of all configurations are very similar and only depend on the charging voltage level. As expected energy factors ΔE related to 1 kV IEC discharge are quadratic to the charging voltage factor. This is also true for transmission line 2 if no protection device is connected. For 8 kV discharge about 240 nJ were simulated at node N4. With protection element the voltage and current peaks can exceed 200 V and 4 A. Simulated energies are higher than 600 nJ. At this energy level IC failure is simulated for 1 kV and 2 kV HBM scaled IC inputs.

Termination at N2	**V_{charge} [kV]**	**V_{max} [V]**	**I_{max} [A]**	**E [µJ]**	**$E/E_{1\ kV}$**
No ESD protection	1	139,97	2,80	8,24	1
Varistor CT0603K14G	1	139,5	2,79	8,24	1
TVS Diode GBLCSC05C	1	139,53	2,79	8,23	1
Capacitor 10nF	1	139,76	2,79	8,24	1
No ESD protection	2	279,93	5,60	32,96	4
Varistor CT0603K14G	2	279	5,58	32,96	4
TVS Diode GBLCSC05C	2	281,21	5,62	33,00	4
Capacitor 10nF	2	279,52	5,59	32,96	4
No ESD protection	4	559,87	11,20	131,84	16
Varistor CT0603K14G	4	558	11,16	131,84	16

TVS Diode GBLCSC05C	4	567,61	11,35	132,48	16
Capacitor 10nF	4	559,03	11,18	131,84	16
No ESD protection	8	1119,7	22,39	527,35	64
Varistor CT0603K14G	8	1116	22,32	527,36	64
TVS Diode GBLCSC05C	8	1135,7	22,71	533,71	64
Capacitor 10nF	8	1118,1	22,36	527,36	64

Table 31: Simulated quantities at node N2 on PCB trace 1

Termination at N4	V_{charge} [kV]	V_{max} [V]	I_{max} [A]	E [nJ]	$E/E_{1\ kV}$
No ESD protection	1	14,47	0,29	3,73	1
Varistor CT0603K14G	1	22,10	0,44	13,05	3,5
TVS Diode GBLCSC05C	1	17,44	0,34	4,46	1,19
Capacitor 10nF	1	25,92	0,51	14,06	3,77
No ESD protection	2	28,94	0,58	14,92	4
Varistor CT0603K14G	2	44,20	0,88	52,22	14,03
TVS Diode GBLCSC05C	2	42,50	0,85	28,44	7,64
Capacitor 10nF	2	51,85	1,03	56,26	15,12
No ESD protection	4	57,87	1,16	59,67	16
Varistor CT0603K14G	4	88,41	1,76	207,72	55,83
TVS Diode GBLCSC05C	4	94,02	1,88	151,57	40,74
Capacitor 10nF	4	103,70	2,07	225,06	60,50
No ESD protection	8	115,75	2,31	238,68	64
Varistor CT0603K14G	8	176,86	3,53	**758,79**	203,97
TVS Diode GBLCSC05C	8	180,98	3,61	**644,33**	173,20
Capacitor 10nF	8	207,40	4,14	**900,24**	242

Table 32: Simulated quantities at node N4 on PCB trace 2

5.4 PCB traces terminated with ICs and one protection element on trace 1

A common topology for electronic control units is analyzed in this section. The transmission lines are both terminated with IC models. Coupled signals are simulated at the IC pin for the case that the ESD event on transmission line 1 is influenced by a protection device.

5.4.1 **Simulation setup**

The simulation setup is shown in Figure 198. PCB trace 1 is terminated with the CANH model and PCB trace 2 with µC DATA model. Terminations at nodes N1 and N3 were connected to 1 kΩ resistors. ESD protection elements were connected to node N1. The IEC generator discharge is simulated at node N1. The same parameters for the coupled PCB traces are used as described in chapter 4 regarding the cross-talk section on the demonstrator PCB.

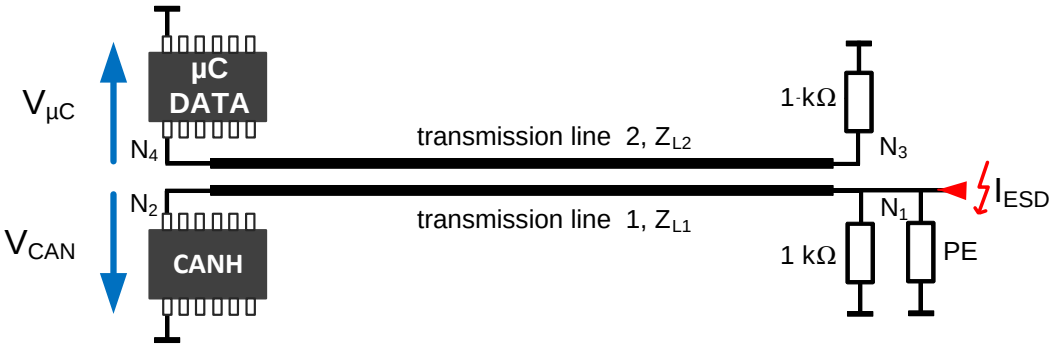

Figure 198: Simulation setup with ICs and protection elements on PCB trace 1

5.4.2 **Simulation results**

Simulated current and voltage waveforms at the CANH and µC pin are given for 1 kV and 8 kV charging voltage in Figure 199 to Figure 206. High voltage and current peaks are obtained for the reference curve because no protection device is connected. The curves indicated with capacitor, varistor and diode are much lower and only about 25 % of the reference amplitudes can be simulated for the 8 kV IEC discharge. All waveforms simulated at the DATA pin are dominated by reflections on the conductors and clamping effects. Similar maximum voltage amplitudes around 3 V are simulated for 1 kV and 8 kV discharges because of clamping behavior of the IC. Current amplitudes are different for the selected levels of charging voltage.

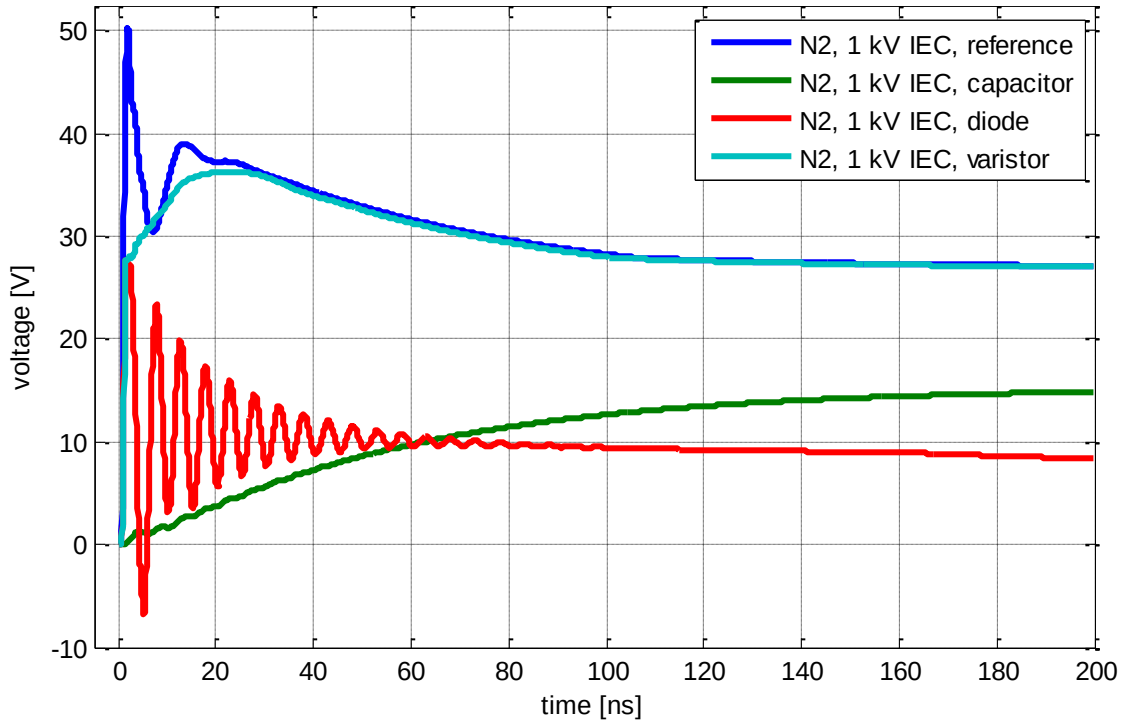

Figure 199: Simulated voltage at CANH pin and 1 kV IEC discharge at node N2

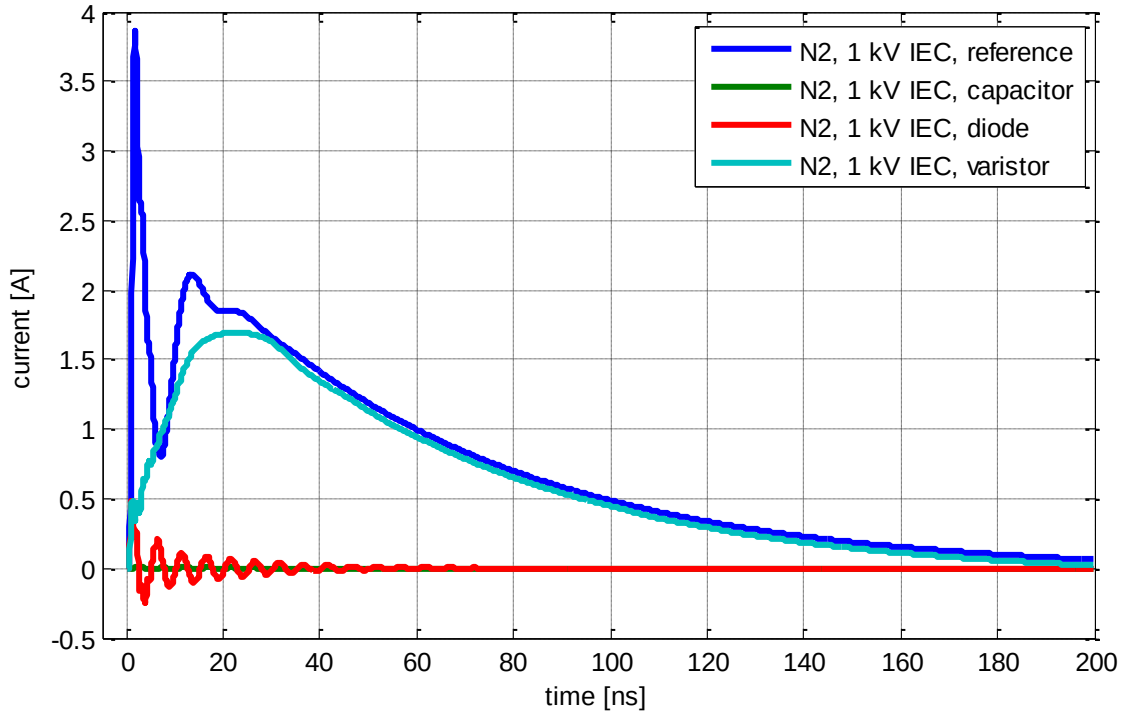

Figure 200: Simulated current through CANH pin and 1 kV IEC discharge at node N2

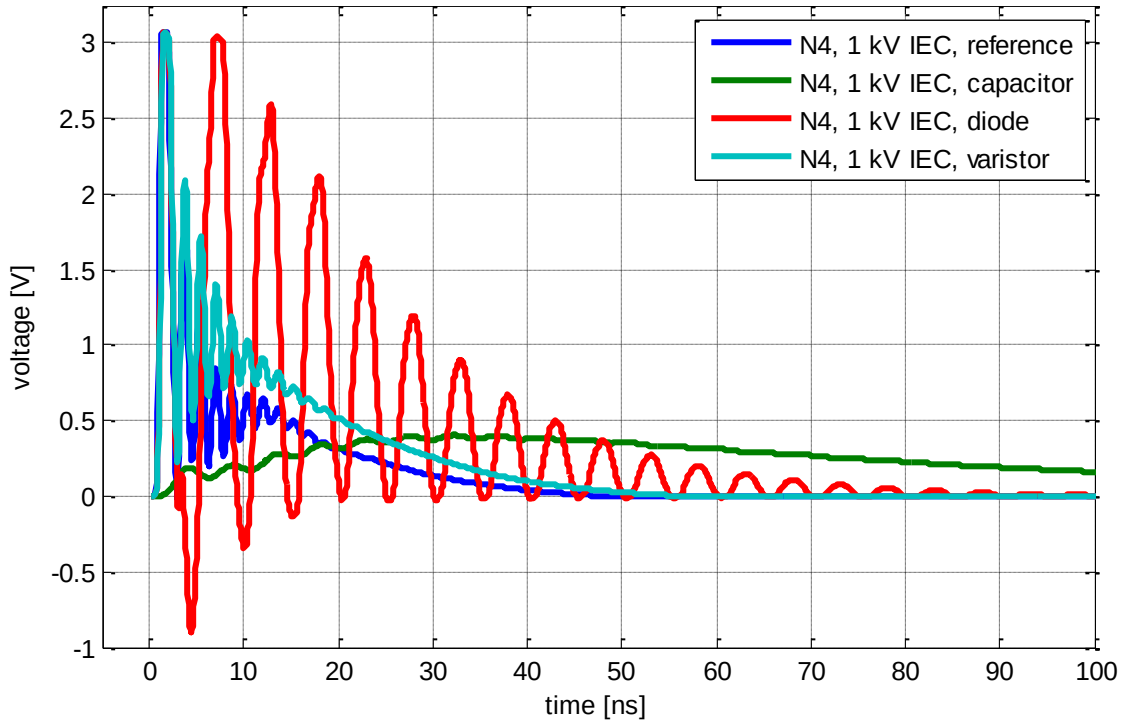

Figure 201: Simulated voltage at µC DATA pin and 1 kV IEC discharge at node N4

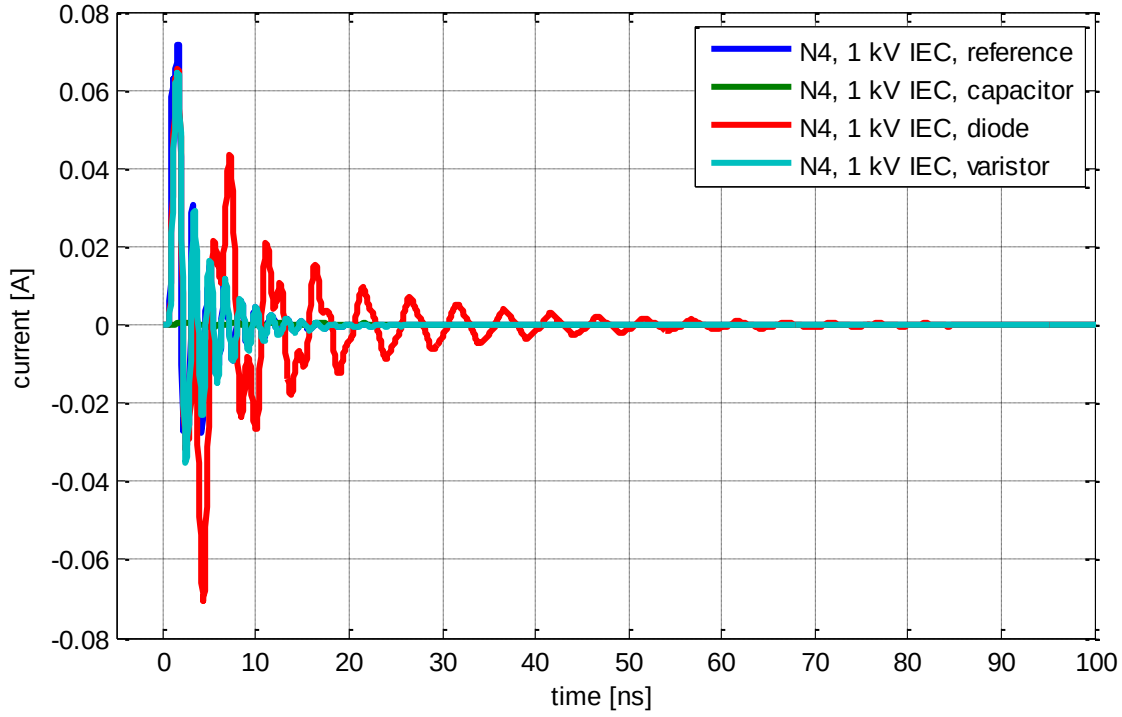

Figure 202: Simulated current through µC DATA pin and 1 kV IEC discharge at node N4

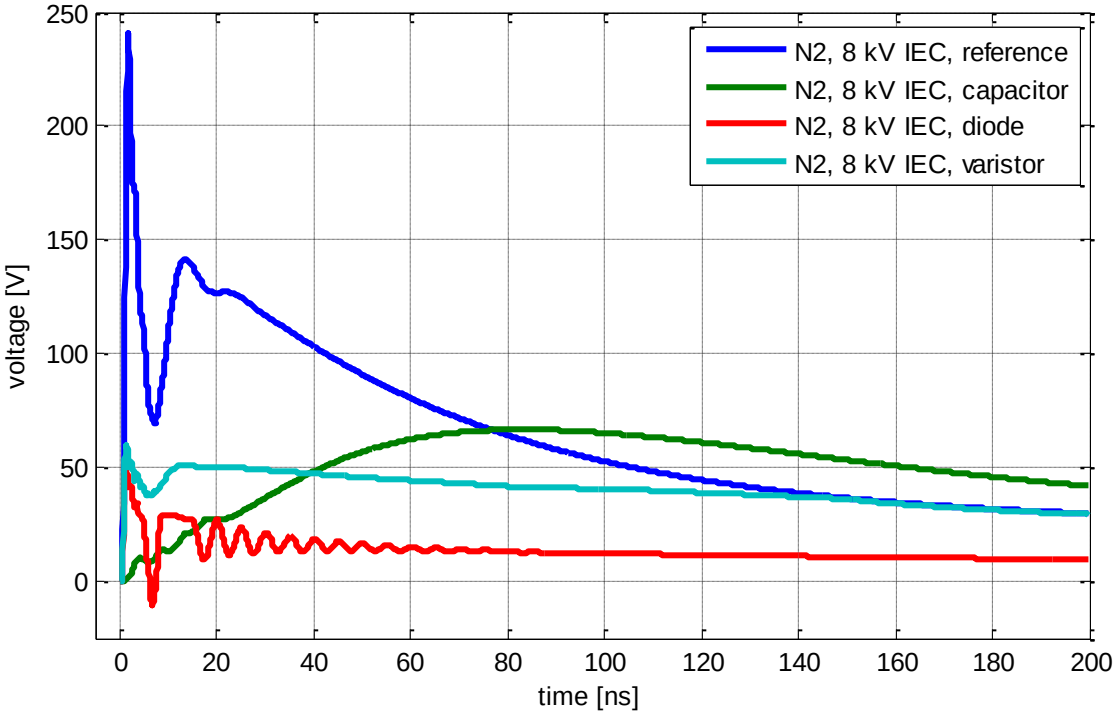

Figure 203: Simulated voltage at CANH pin and 8 kV IEC discharge at node N2

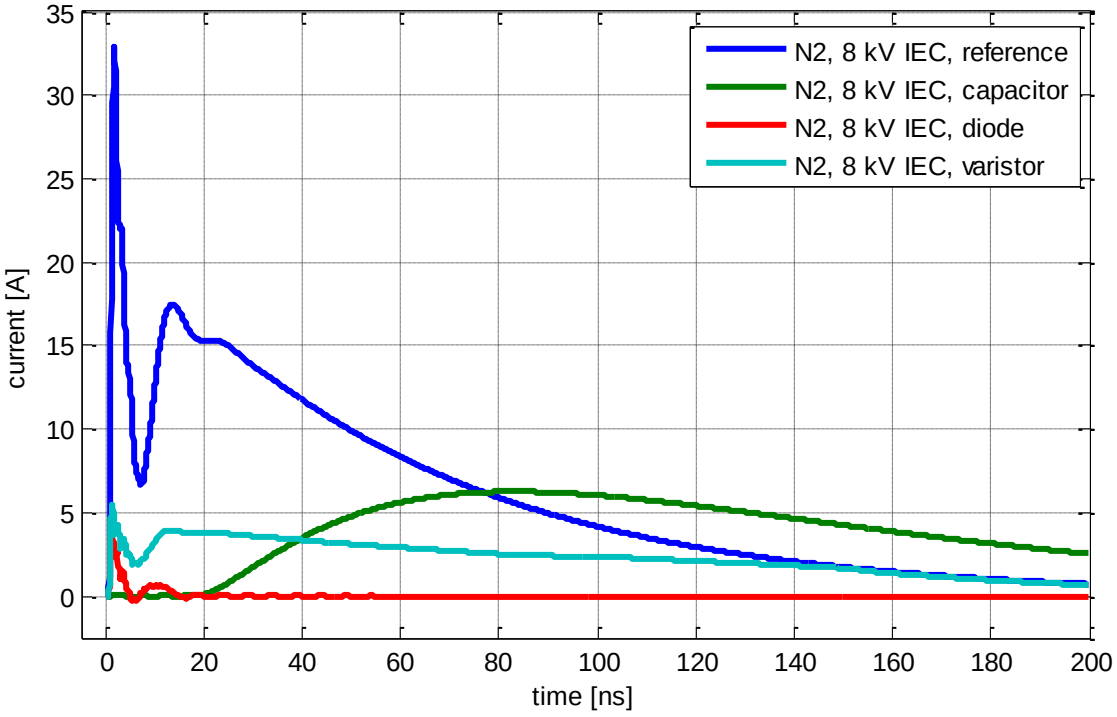

Figure 204: Simulated current through CANH pin and 1 kV IEC discharge at node N2

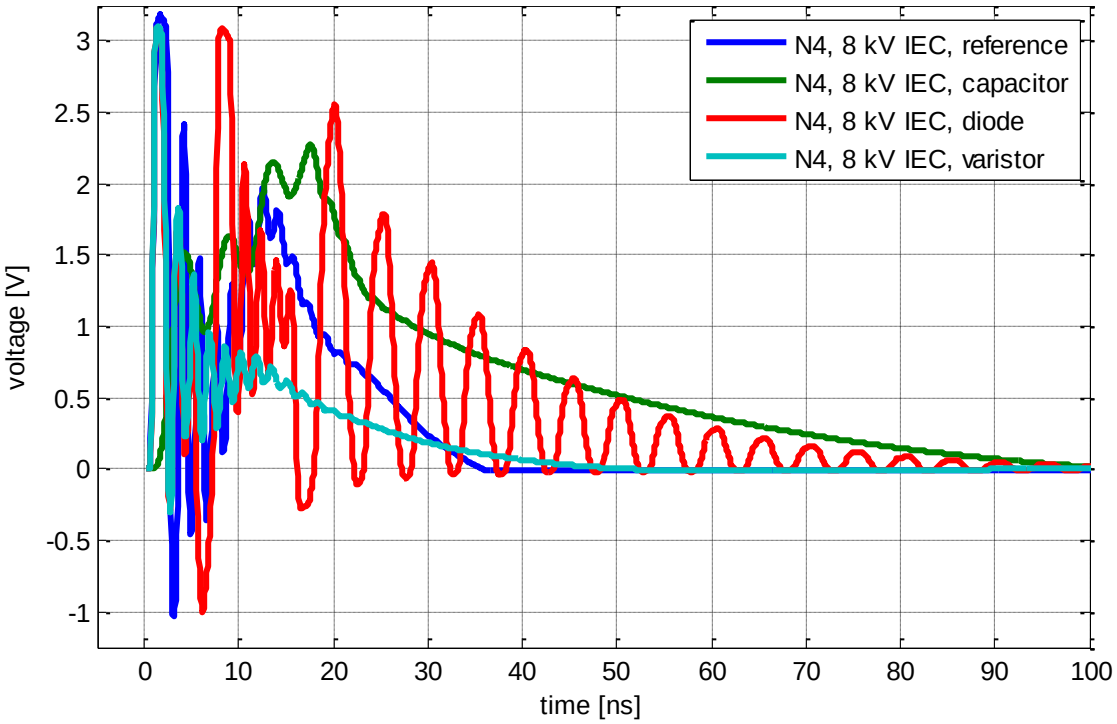

Figure 205: Simulated voltage at µC DATA pin and 8 kV IEC discharge at node N4

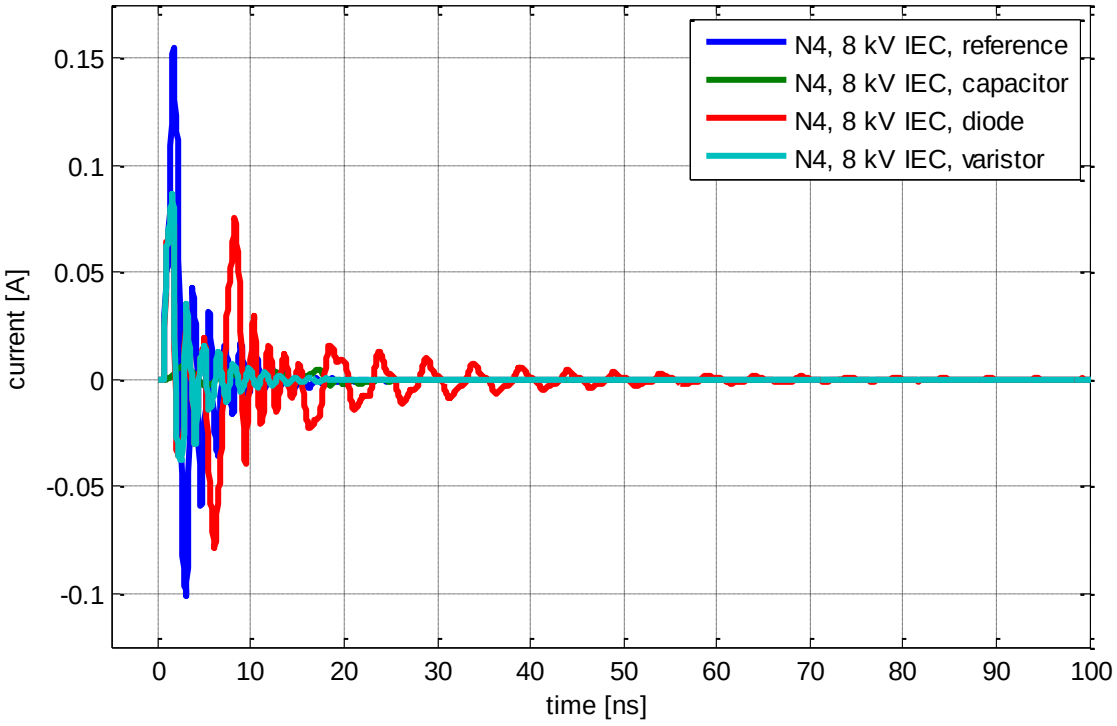

Figure 206: Simulated current through µC DATA pin and 8 kV IEC discharge at node N4

Maximum current and voltage amplitudes and the calculated energies are given in Table 33 and Table 34. If factors ΔE at node N2 are compared for different charging voltages, the TVS diode can be figured out as the most effective protection device. For the 8 kV IEC discharge only about 8 % of the energy is simulated at the CANH pin compared to the 1 kV reference value. Significant differences between the

maximum amplitudes are obtained. As mentioned before peak amplitudes at the µC pin are moderate. The reference curve reaches 150 mA. Because the rise time and pulse shape is attenuated on PCB trace 1 only very small coupling energies of less than 1 nJ are obtained for the analyzed topology.

PE at N1	V_{charge} [kV]	V_{max} [V]	I_{max} [A]	E [µJ]	$E/E_{1\ kV}$
No ESD protection	1	50,23	3,86	4,8	1
Varistor CT0603K14G	1	36,2	1,69	3,91	0,81
TVS Diode GBLCSC05C	1	27,67	0,48	0,04	0,01
Capacitor 10nF	1	14,87	0,007	0,002	4,37e-4
No ESD protection	2	77,65	8,03	12,51	2,6
Varistor CT0603K14G	2	40,02	2,25	7,60	1,58
TVS Diode GBLCSC05C	2	30,60	0,90	0,06	0,01
Capacitor 10nF	2	27,96	0,44	0,66	0,14
No ESD protection	4	132,09	16,37	36,04	7,5
Varistor CT0603K14G	4	43,52	2,78	12,35	2,57
TVS Diode GBLCSC05C	4	36,99	1,88	0,14	0,03
Capacitor 10nF	4	40,63	2,35	10,61	2,21
No ESD protection	8	240,93	32,95	115,52	24,06
Varistor CT0603K14G	8	60,07	5,41	19,59	4,08
TVS Diode GBLCSC05C	8	49,6	3,85	0,41	0,08
Capacitor 10nF	8	66,69	6,26	46,49	9,68

Table 33: Simulated quantities at node N2 for configuration with ICs and an protection element

PE at N1	V_{charge} [kV]	V_{max} [V]	I_{max} [A]	E [nJ]	$E/E_{1\ kV}$
No ESD protection	1	3,09	0,08	0,26	1
Varistor CT0603K14G	1	3,06	0,06	0,25	0,96
TVS Diode GBLCSC05C	1	3,07	0,07	0,54	2,07
Capacitor 10nF	1	0,4	7,5e-4	0,002	0,01
No ESD protection	2	3,09	0,08	0,26	1
Varistor CT0603K14G	2	3,07	0,07	0,26	1
TVS Diode GBLCSC05C	2	3,07	0,07	0,67	2,57
Capacitor 10nF	2	0,80	0,001	0,01	0,03
No ESD protection	4	3,12	0,10	0,34	1,36
Varistor CT0603K14G	4	3,07	0,07	0,27	1,03
TVS Diode GBLCSC05C	4	3,08	0,10	0,76	2,92
Capacitor 10nF	4	1,57	0,003	0,03	0,12
No ESD protection	8	3,18	0,15	0,65	2,6
Varistor CT0603K14G	8	3,09	0,09	0,28	1,07
TVS Diode GBLCSC05C	8	3,08	0,08	0,77	2,96
Capacitor 10nF	8	2,27	0,006	0,07	0,26

Table 34: Simulated quantities at node N4 for configuration with ICs and an protection element

5.5 PCB traces terminated with ICs and protection elements

For the topology in section 5.4 no critical amplitudes were simulated. Previous measurement and simulation results have shown that coupled peak voltage and current can be higher if a protection device is connected to PCB trace 2.

5.5.1 Simulation setup

In the simulation setup in Figure 207 an ESD protection device was added at node N3. The signals at CANH and DATA pin are simulated for IEC ESD generator discharges at node N1 for different charging voltages.

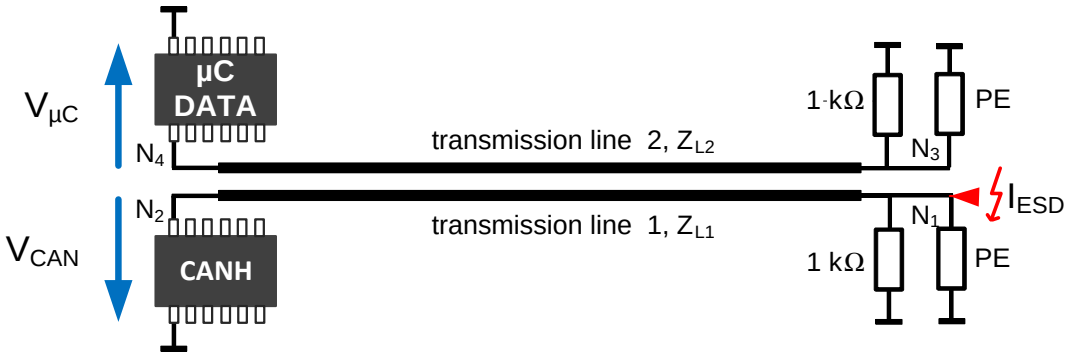

Figure 207: Simulation setup with ICs and protection elements on both transmission lines

5.5.2 **Simulation results**

Simulated current and voltage shapes at node N2 and N4 are shown in Figure 208 to Figure 215. Almost the same waveforms are simulated at the CANH pin compared to section 5.4 because the feedback from PCB trace 2 to trace 1 is very low. The ringing observed in the waveforms at the µC pin is not attenuated by the protection device at node N3. Current and voltage peak amplitudes increase compared to the curves in the previous section.

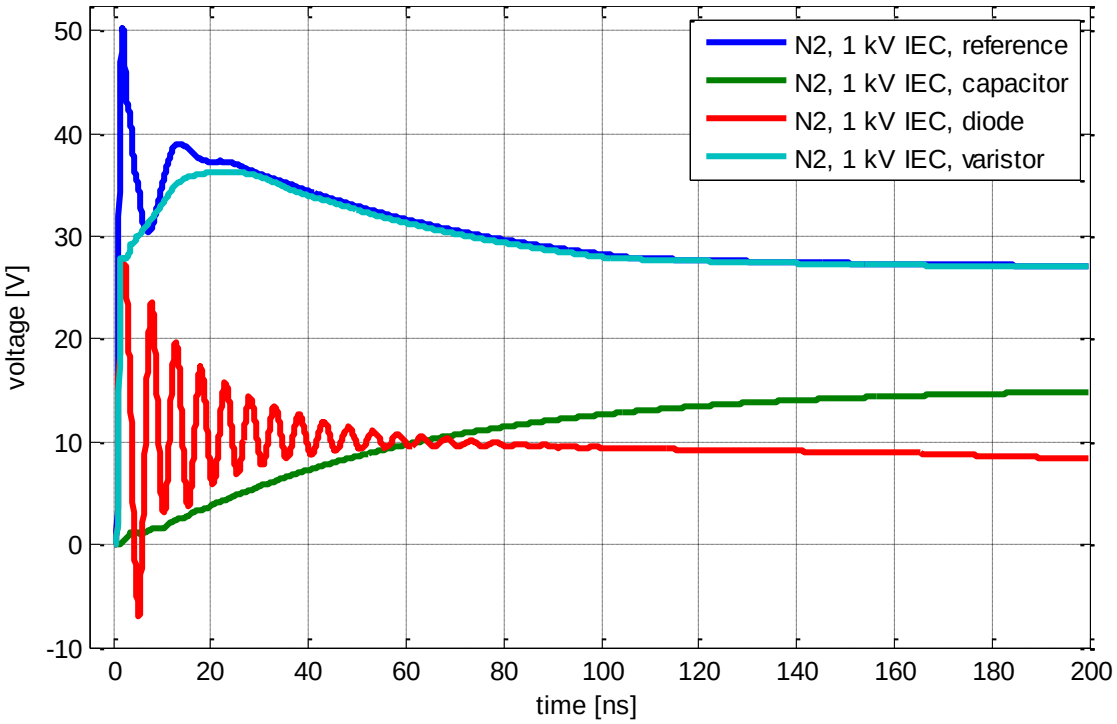

Figure 208: Simulated voltage at CANH pin for 1 kV IEC generator discharge

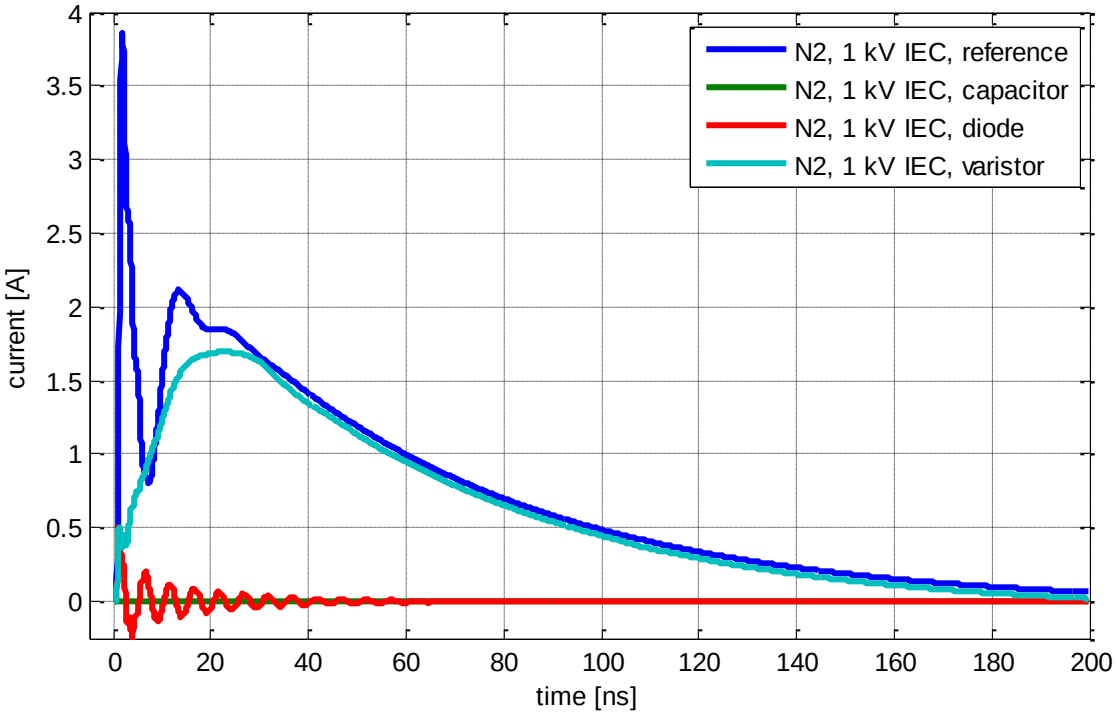

Figure 209: Simulated current through CANH pin for 1 kV IEC generator discharge

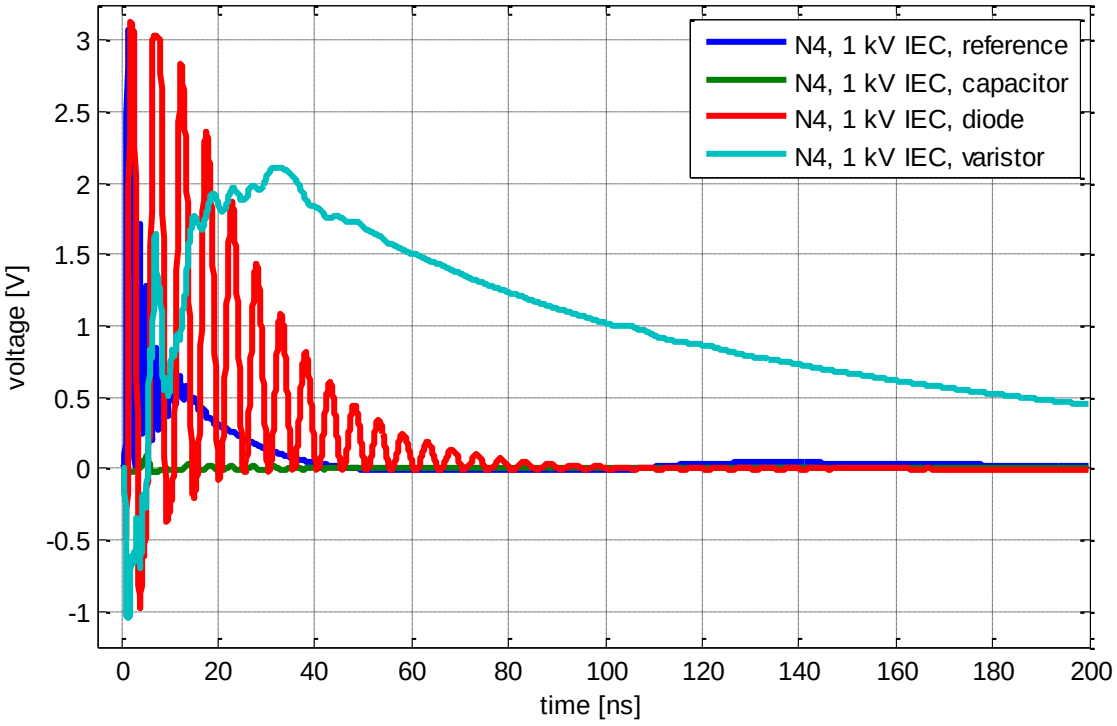

Figure 210: Simulated voltage at µC DATA pin for 1 kV discharge on TL 2

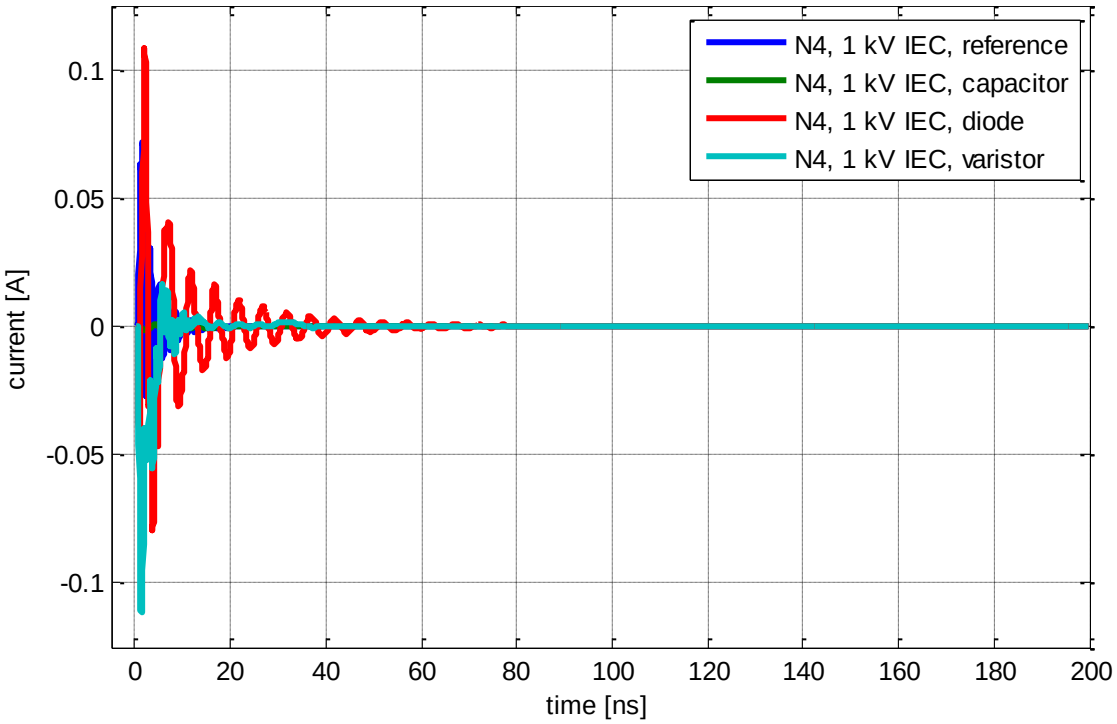

Figure 211: Simulated current through µC DATA pin for 1 kV discharge on TL 2

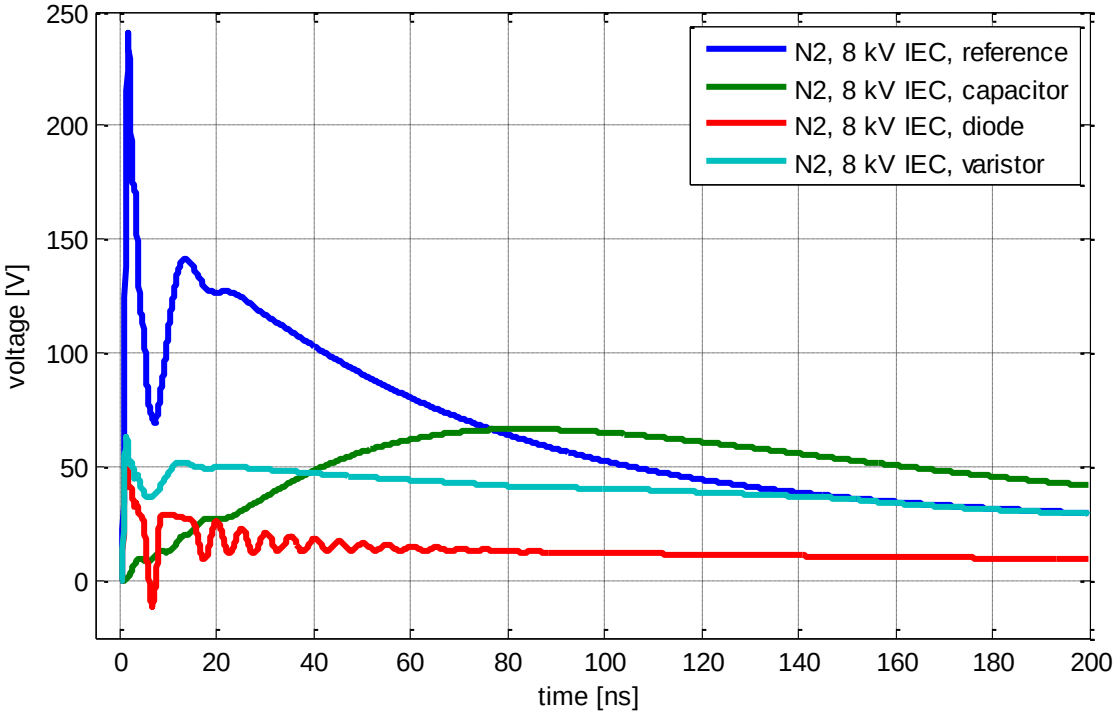

Figure 212: Simulated voltage at CANH pin for 8 kV IEC generator discharge

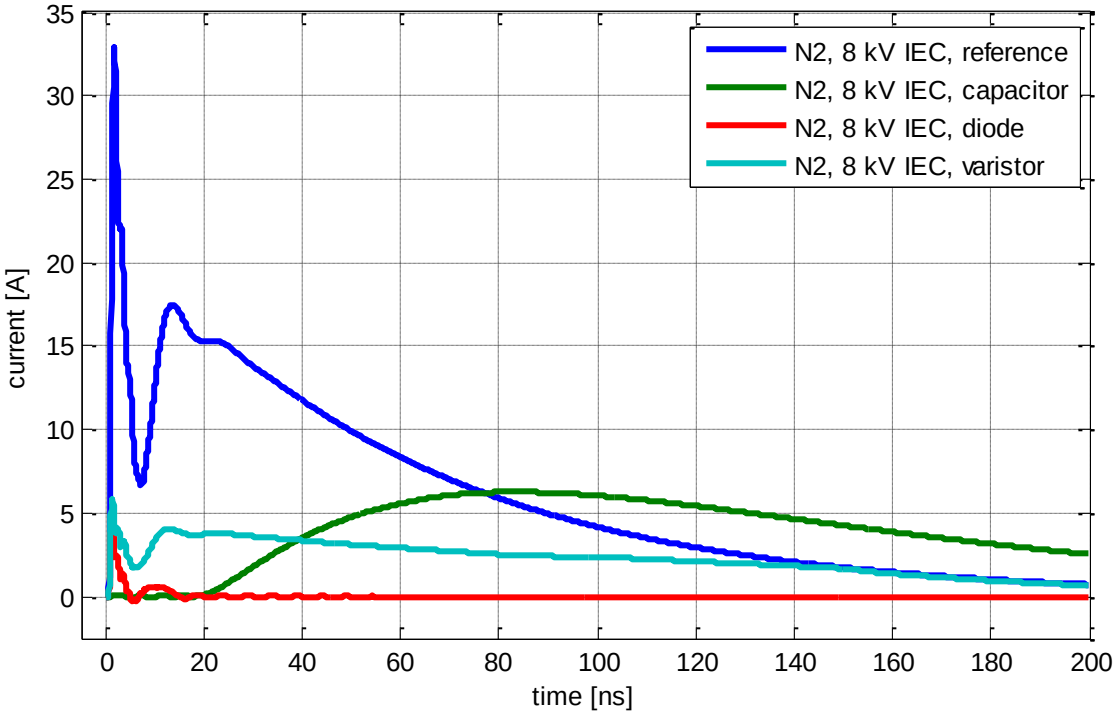

Figure 213: Simulated current through CANH pin for 8 kV IEC generator discharge

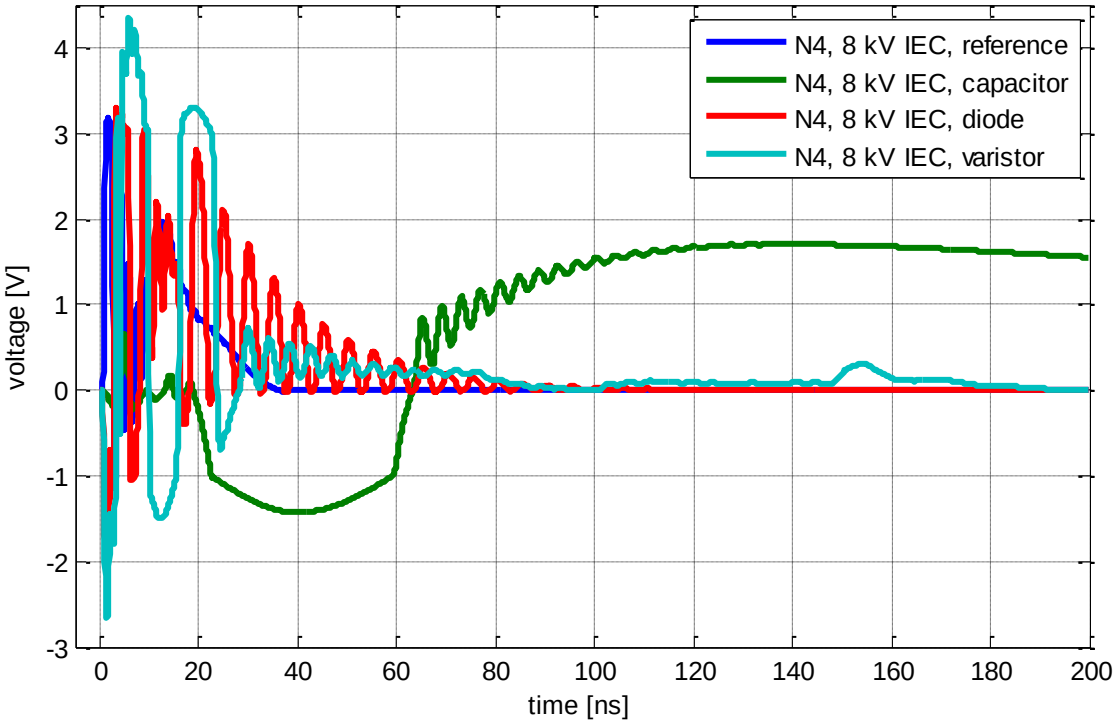

Figure 214: Simulated voltage at µC DATA pin for 8 kV discharge on TL 2

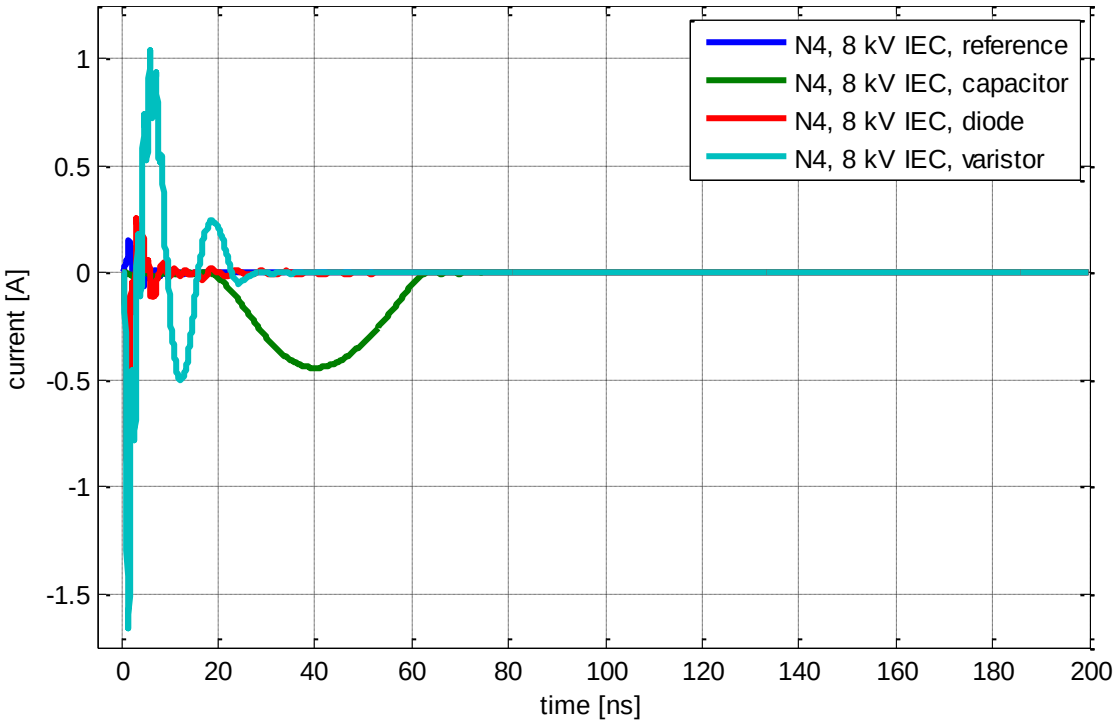

Figure 215: Simulated current through µC DATA pin for 8 kV discharge on TL 2

Termination at N1 and N3	V_{charge} [kV]	V_{max} [V]	I_{max} [A]	E [µJ]	$E/E_{1\ kV}$
No ESD protection	1	50,23	3,86	4,8	1
Varistor CT0603K14G	1	36,27	1,69	3,91	0,81
TVS Diode GBLCSC05C	1	27,71	0,50	0,036	7,6e-3
Capacitor 10nF	1	14,87	0,007	0,002	43e-3
No ESD protection	2	77,65	8,03	12,51	2,6
Varistor CT0603K14G	2	40,02	2,25	7,60	1,58
TVS Diode GBLCSC05C	2	30,84	0,94	0,064	13,3e-3
Capacitor 10nF	2	27,95	0,44	0,66	0,14
No ESD protection	4	132,09	16,37	36,04	7,5
Varistor CT0603K14G	4	43,52	2,8	12,35	2,57
TVS Diode GBLCSC05C	4	37,77	2,00	0,14	0,03
Capacitor 10nF	4	40,63	2,35	10,60	2,2
No ESD protection	8	240,93	32,95	115,52	24,06
Varistor CT0603K14G	8	62,91	5,87	19,61	4,08
TVS Diode GBLCSC05C	8	51,56	4,14	0,42	87,5e-3
Capacitor 10nF	8	66,70	6,26	46,46	9,67

Table 35: Simulated quantities at node N2 with IC models and ESD protection elements

Termination at N1 and N3	V_{charge} [kV]	V_{max} [V]	I_{max} [A]	E [nJ]	$E/E_{1\ kV}$
No ESD protection	1	3,09	0,08	0,26	1
Varistor CT0603K14G	1	2,11	0,11	0,23	0,88
TVS Diode GBLCSC05C	1	3,12	0,10	0,75	2,88
Capacitor 10nF	1	0,087	0,002	2,6e-4	1e-3
No ESD protection	2	3,09	0,08	0,26	1
Varistor CT0603K14G	2	3,12	0,33	1,55	5,96
TVS Diode GBLCSC05C	2	3,13	0,11	0,94	3,61
Capacitor 10nF	2	0,17	0,012	0,04	0,16
No ESD protection	4	3,12	0,10	0,34	1,36
Varistor CT0603K14G	4	3,52	0,78	6,43	24,73
TVS Diode GBLCSC05C	4	3,20	0,36	1,51	5,8
Capacitor 10nF	4	1,0	0,07	1,30	5
No ESD protection	8	3,18	0,15	0,65	2,6
Varistor CT0603K14G	8	4,34	1,66	23,65	90,96
TVS Diode GBLCSC05C	8	3,30	1,00	2,82	10,84
Capacitor 10nF	8	1,70	0,44	15,29	58,8

Table 36: Simulated quantities at node N4 with IC models and ESD protection elements

Simulated values at the CANH and µC pin are given in Table 35 and Table 36. The coupled energy from a 1 kV reference discharge without ESD protection is expressed by the factor ΔE. In case of the TVS diode about 3 times more coupling energy was simulated for a 1 kV discharge at node N4. The maximum coupling energy was simulated with varistor and 8 kV charging voltage to about 25 nJ.

5.6 PCB trace 2 terminated with ESD protection element

In section 5.3 significant peak values were simulated for a configuration with 50 Ω resistors at nodes N2 and N4. The loads are replaced by IC models and currents and voltages are simulated for IEC generator discharges.

5.6.1 **Simulation setup**

In the simulation setup the protection element at node N1 is removed. A sketch is shown in Figure 216. PCB parameters are kept from the previous section.

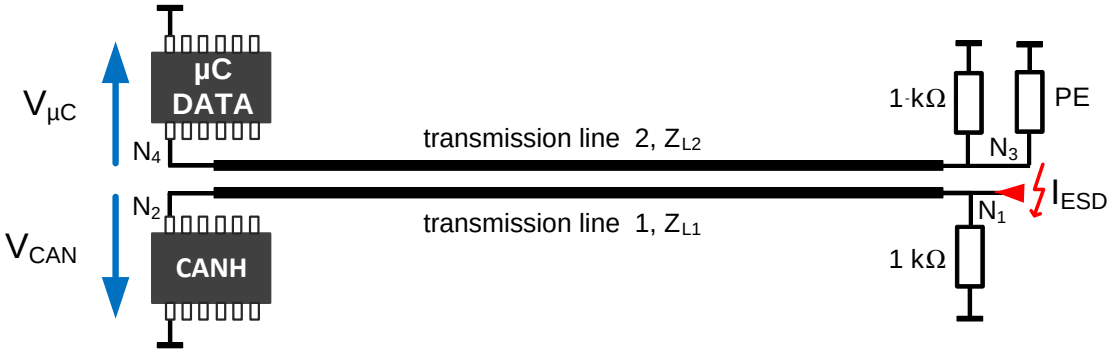

Figure 216: Simulation setup for worst case configuration

5.6.2 Simulation results

No ESD protection element was connected to trace 1. Simulated voltage and currents are very similar to the reference voltage and current shapes at the CANH pin shown in Figure 208, Figure 209, Figure 212 and Figure 213. Waveforms at the µC pin are compared in Figure 217 to Figure 220 for 1 kV and 8 kV charging voltage. Peak amplitudes for the coupled signals are higher. About 10 V and 10 A are simulated for the 8 kV discharge. Reflections and clamping effects at different voltage levels are observed.

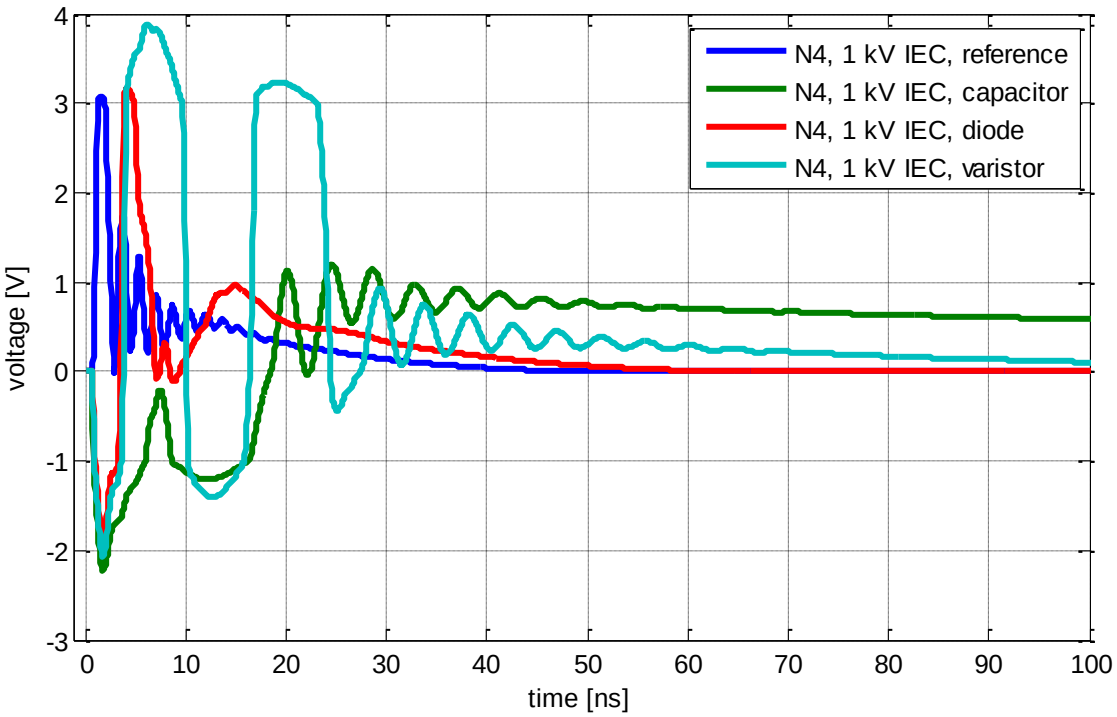

Figure 217: Simulated voltage for 1 kV IEC discharge on node N4 with IC and ESD protection

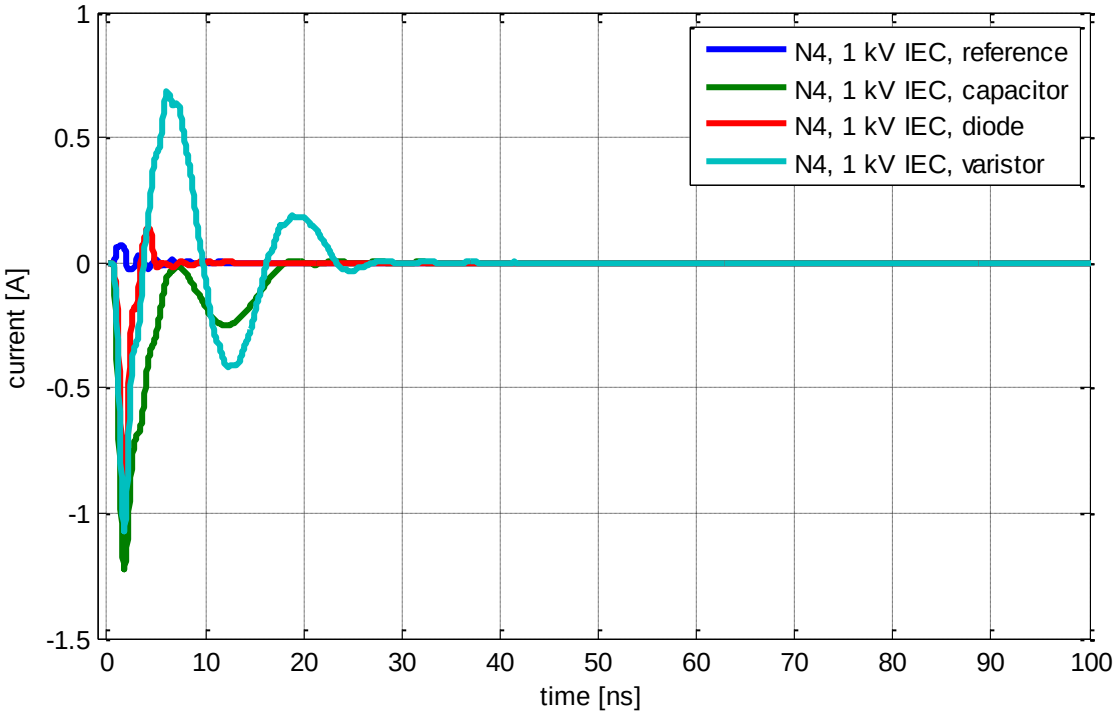

Figure 218: Simulated current for 1 kV IEC discharge on node N4 with IC and ESD protection

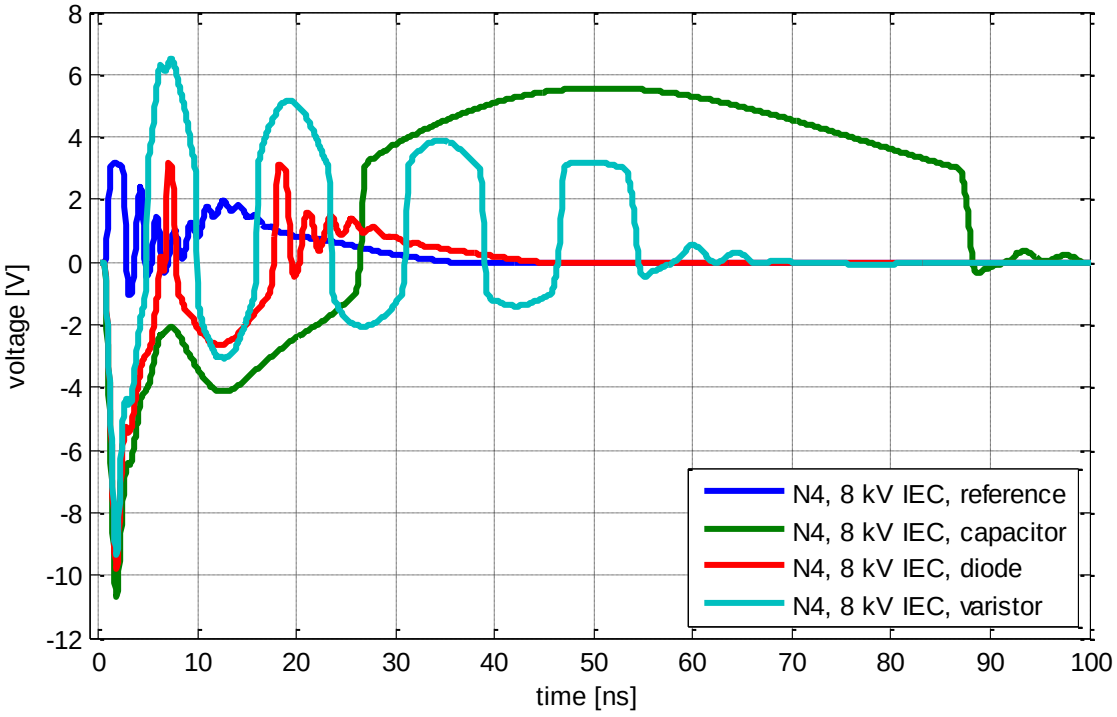

Figure 219: Simulated voltage for 8 kV IEC discharge on node N4 with IC and ESD protection

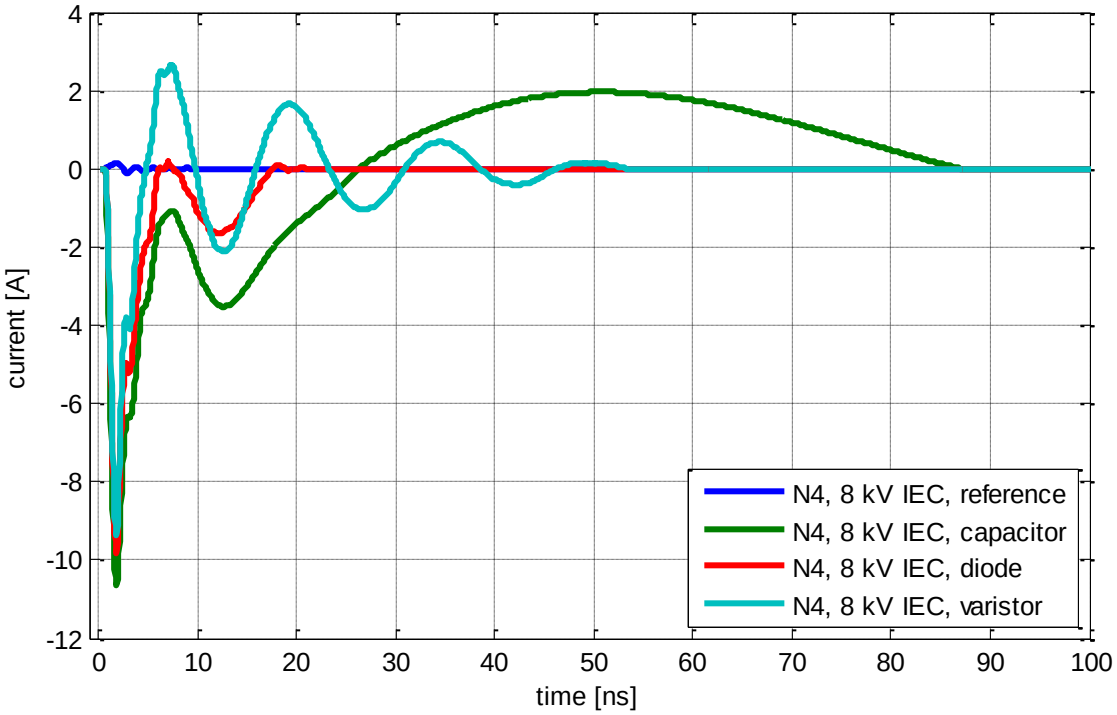

Figure 220: Simulated current for 8 kV IEC discharge on node N4 with IC and ESD protection

Load	V_{charge} [kV]	V_{max} [V]	I_{max} [A]	E [µJ]	$E/E_{1\ kV}$
No ESD protection	1	50,23	3,86	4,8	1
Varistor CT0603K14G	1	50,86	3,95	4,80	1
TVS Diode GBLCSC05C	1	50,77	3,94	4,80	1
Capacitor 10nF	1	50,94	3,97	4,80	1
No ESD protection	2	77,65	8,03	12,51	2,6
Varistor CT0603K14G	2	78,95	8,23	12,51	2,6
TVS Diode GBLCSC05C	2	79,29	8,28	12,52	2,6
Capacitor 10nF	2	79,46	8,33	12,52	2,6
No ESD protection	4	132,09	16,37	36,04	7,5
Varistor CT0603K14G	4	134,83	16,8	36,04	7,5
TVS Diode GBLCSC05C	4	134,88	16,81	36,05	7,5
Capacitor 10nF	4	135,21	16,85	36,06	7,5
No ESD protection	8	240,93	32,95	115,52	24,06
Varistor CT0603K14G	8	246,47	33,82	115,63	24,08
TVS Diode GBLCSC05C	8	246,73	33,86	115,57	24,07
Capacitor 10nF	8	247,22	33,91	115,57	24,07

Table 37: Simulated quantities at node N2 on TL1 at CANH pin

Load	V_{charge} [kV]	V_{max} [V]	I_{max} [A]	E [nJ]	$E/E_{1\ kV}$
No ESD protection	1	3,07	0,07	0,25	1
Varistor CT0603K14G	1	3,88	1,07	16,61	66,44
TVS Diode GBLCSC05C	1	3,16	0,91	2,08	8,32
Capacitor 10nF	1	2,22	1,22	7,17	28,68
No ESD protection	2	3,09	0,08	0,26	1,04
Varistor CT0603K14G	2	4,94	2,26	58,36	233,44
TVS Diode GBLCSC05C	2	3,30	2,20	9,10	36,4
Capacitor 10nF	2	3,44	2,60	25,49	101,96
No ESD protection	4	3,12	0,10	0,34	1,36
Varistor CT0603K14G	4	6,08	4,64	130,30	521,2
TVS Diode GBLCSC05C	4	5,06	4,73	36,65	146,6
Capacitor 10nF	4	5,49	5,28	137,19	548,76
No ESD protection	8	3,18	0,15	0,65	2,6
Varistor CT0603K14G	8	9,37	9,36	227,69	910,76
TVS Diode GBLCSC05C	8	9,81	9,80	151,46	605,84
Capacitor 10nF	8	10,66	10,66	**692,30**	2769

Table 38: Simulated quantities at node N4 on TL2 at µC DATA pin

Peak values and energies for the described configuration are compared in Table 37 and Table 38. Maximum voltage, current and energy can be simulated if conductor 2 is protected by 10 nF capacitor. The dissipated energy increases by factor 3 compared to the configuration with varistor. Two of three IC models scaled to 1 kV HBM testing level would fail due to the high energy of about 700 nJ.

5.7 Simulation with different PCB traces parameter sets

The influence of the PCB trace geometry parameters on coupling is analyzed. In section 2.2 the parameters Z_{even} and Z_{odd} were introduced, both can be derived from the L and C matrices from the chosen transmission line model for PCB modeling. Z_{even} is calculated from the common mode impedance Z_{com} multiplied by factor 2. Z_{odd} is obtained from the differential mode impedance Z_{diff} divided by factor 2. Z_{diff} is specified as impedance, if the waves on parallel transmission lines propagate in the opposite direction. Z_{com} forms the impedance of the conductors for current waves propagating in the same direction.

In Figure 83 and Figure 84 in chapter 4 the even and odd impedances of the stripline transmission line model were calculated with the TXLINE tool. The input parameters are based on the dimensions of the cross-talk section on the demonstrator PCB.

In Table 39 even and odd impedances were calculated under variation of the dimension of a single structural stripline parameter. The small arrow behind a value indicates if a parameter increases or decreases compared to the reference value. Z_{even} and Z_{odd} are derived from the "per unit length" parameters, the L and C matrices, i.e. the length of the transmission line has no impact.

Parameter	**Variation**	**Z_{even}**	**Z_{odd}**
Reference	**-**	**104,4 Ω**	**53,8 Ω**
Gap	0,3 mm (↓)	107,8 Ω (↑)	47,8 Ω (↓)
Width	0,5 mm (↓)	152,2 Ω (↑)	71,3 Ω (↑)
Height	0,5 mm (↓)	47,0 Ω (↓)	37.9 Ω (↓)
Permittivity	4,2 (↓)	108,2 Ω (↑)	55,6 Ω (↑)
Thickness	10 µm (↓)	106,7 Ω (↑)	54,3 Ω (↑)

Table 39: Impact of variation of stripline dimensions on line impedance

Waveforms with variation of Z_{even} and Z_{odd} impedances for the topology shown in Figure 184 are simulated. The transmission lines are terminated with 50 Ω and 1 kΩ resistors. The energy of a 2 kV IEC generator discharge is calculated from the waveforms at the 50 Ω resistors at both conductors. Variation of even and odd impedances on the energy is analyzed in Figure 221 and Figure 222. The coupling energy on conductor 2 at node N4 is maximal for the biggest difference between Z_{even} and Z_{odd} values. On transmission line 1 the maximum energy is simulated for Z_{even} and Z_{odd} values matching the single line impedance.

The results shown in Figure 223 and Figure 224 were simulated by replacing the 50 Ω resistors with CANH and the µC DATA model according to Figure 189. The curve of the coupled energy at the DATA pin becomes maximum for Z_{odd} = 27 Ω and Z_{even} = 77 Ω.

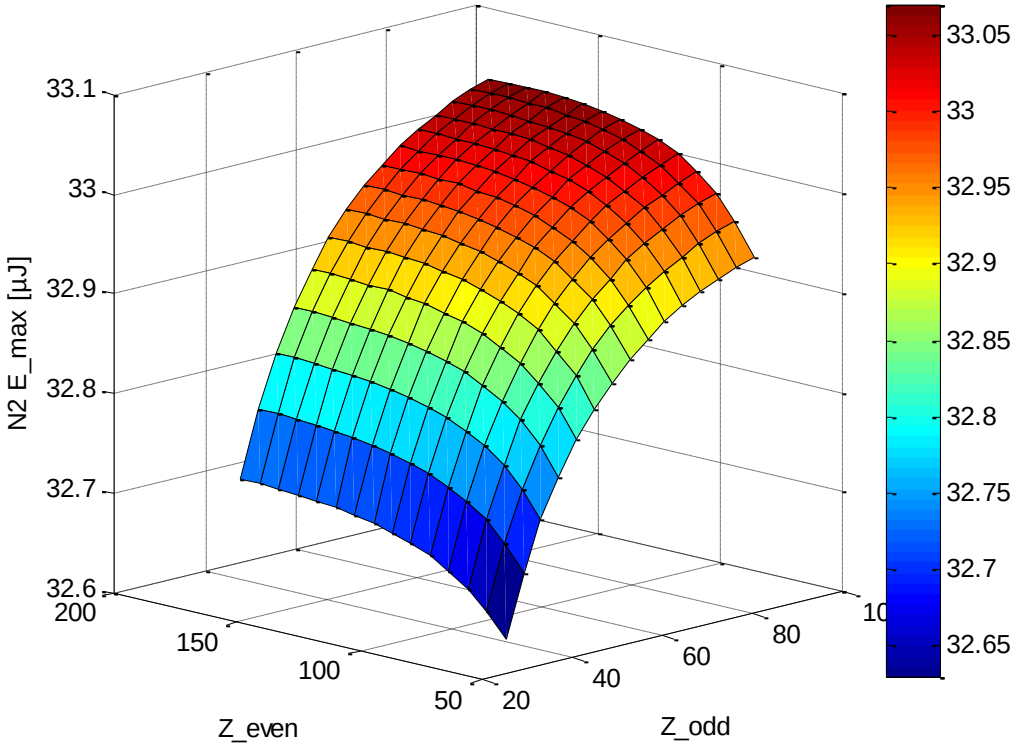

Figure 221: Energy of simulated IEC 2 kV discharge at node N2 over 50 Ω

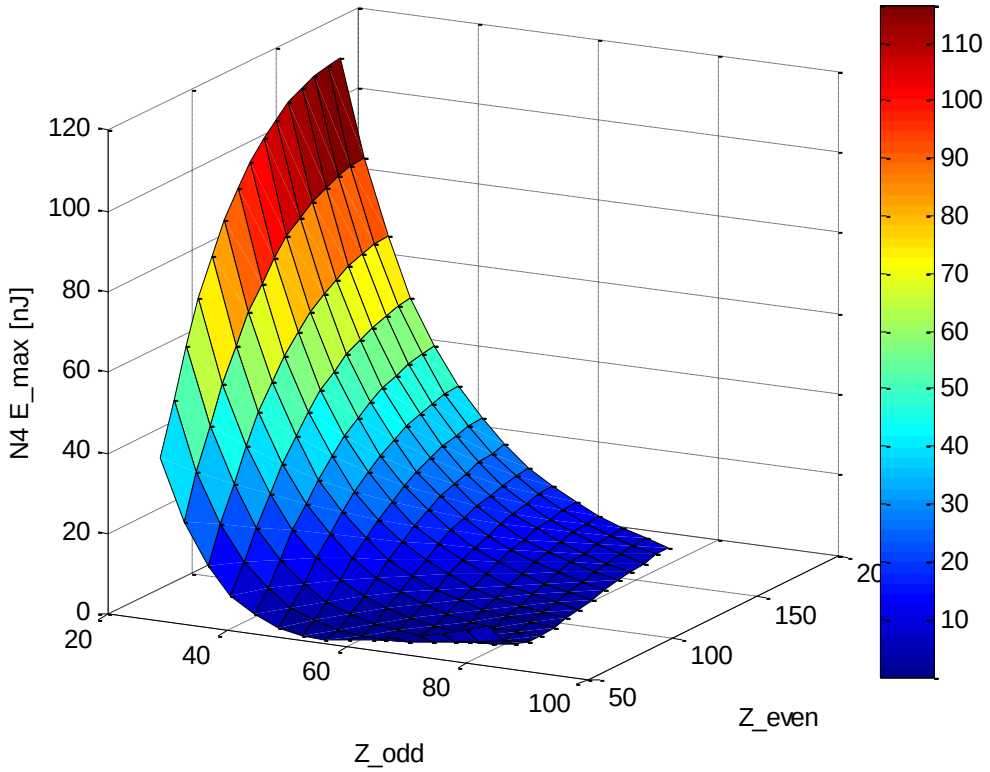

Figure 222: Energy of simulated IEC 2 kV discharge at node N4 over 50 Ω

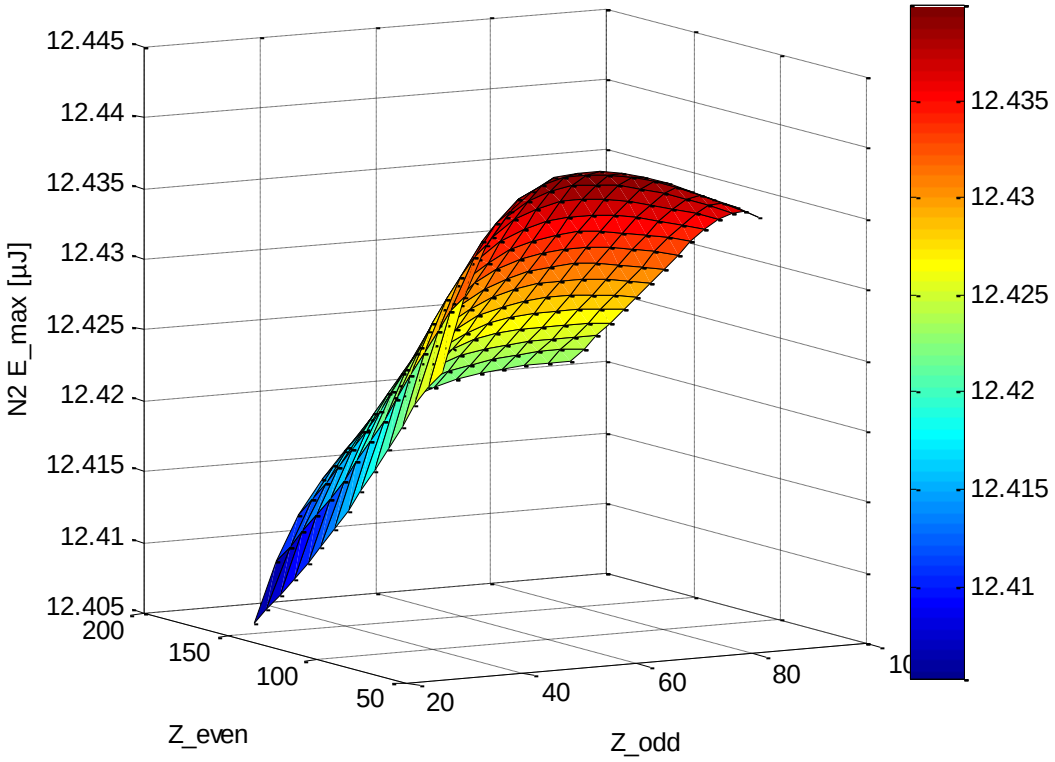

Figure 223: Energy of simulated IEC 2 kV discharge at node N2 at CANH-pin

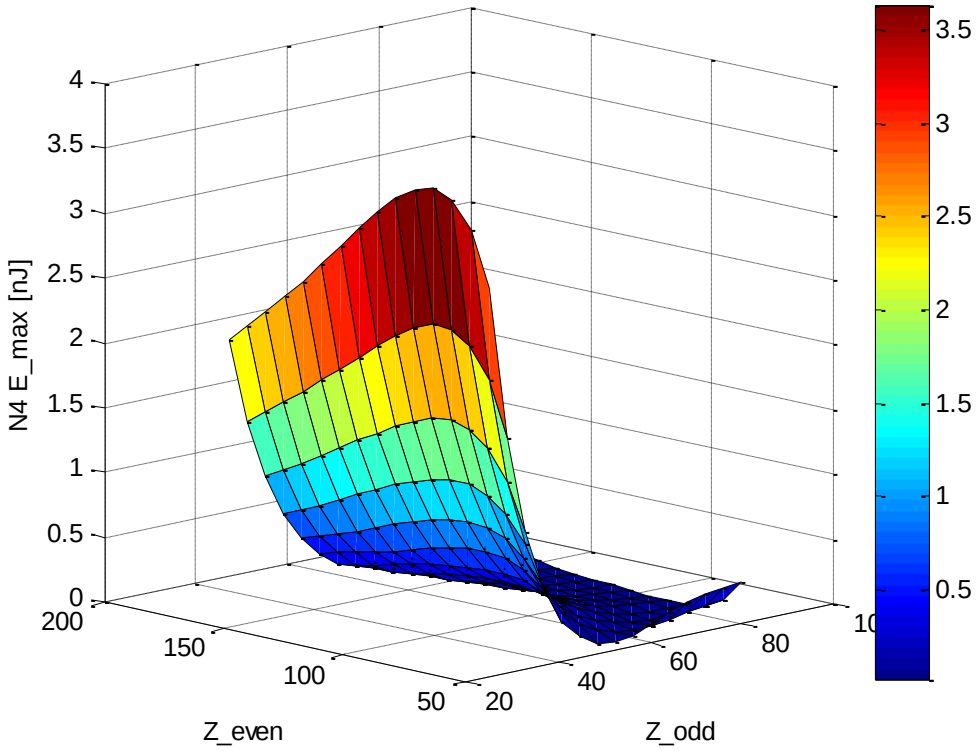

Figure 224: Energy of simulated IEC 2 kV discharge at node N4 at µC Data-pin

The impact of trace parameters on coupled signals was analyzed also directly. Figure 225 shows the simulation setup for traces terminated with resistors where different values for trace length and trace distance were chosen. The IEC ESD generator is discharged at node N1.

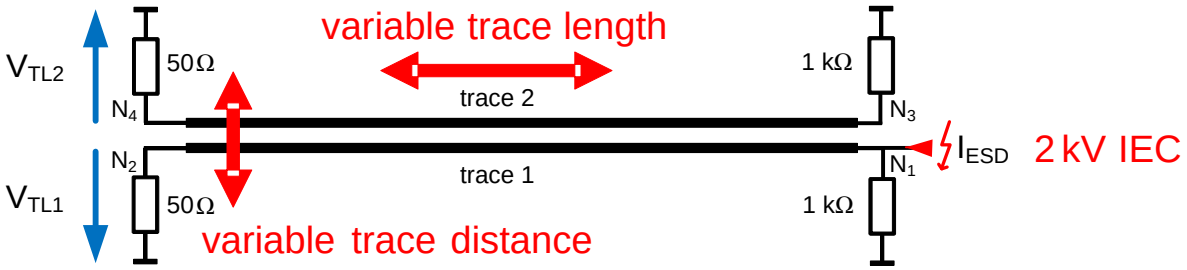

Figure 225: Simulation setup with variable trace length and trace distance for resistors

Voltage and currents are simulated at 50 Ω resistors at node N2 and N4 and energies were calculated. According to Figure 226 a quite stable value of the energy at the trace of the initial discharge is simulated. The effect of variation of trace length and distance can be observed in Figure 227 at node N4. The highest energy was simulated for a short distance and long trace length.

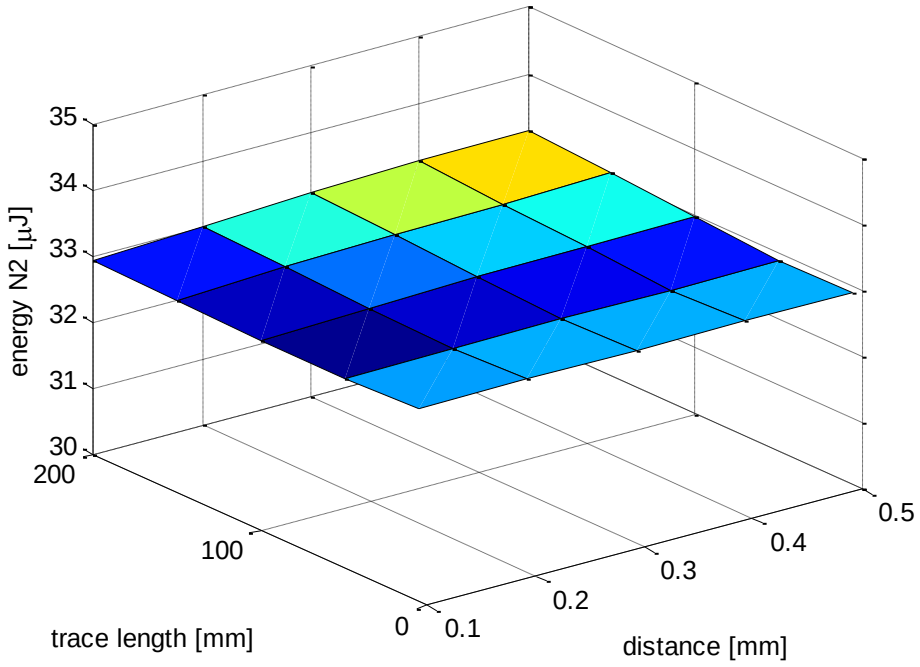

Figure 226: Energy of simulated IEC 2 kV discharge at node N2 over 50 Ω

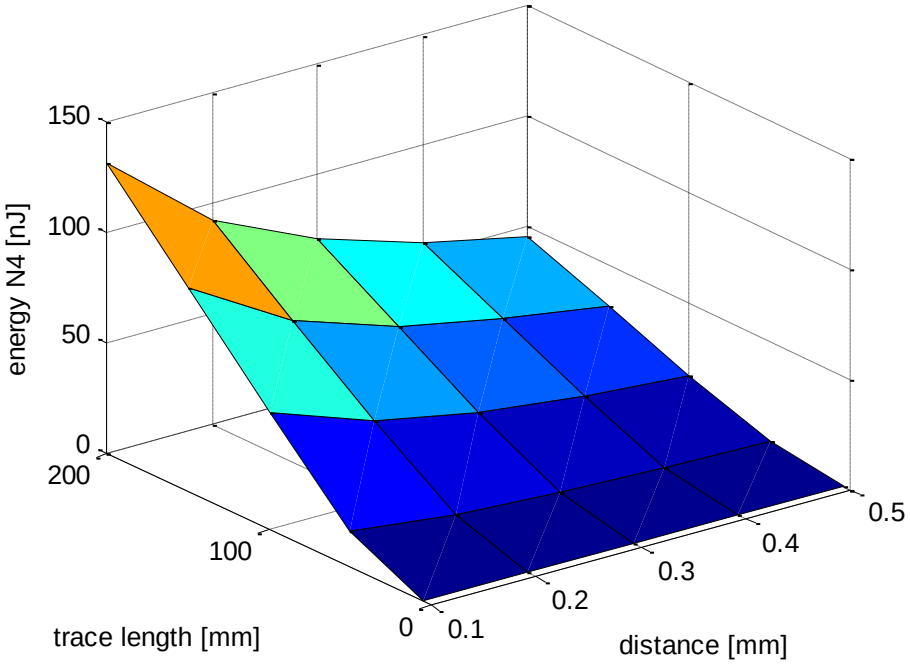

Figure 227: Energy of simulated IEC 2 kV discharge at node N4 over 50 Ω

In the setup shown in Figure 228 the 50 Ω resistors were replaced by IC models.

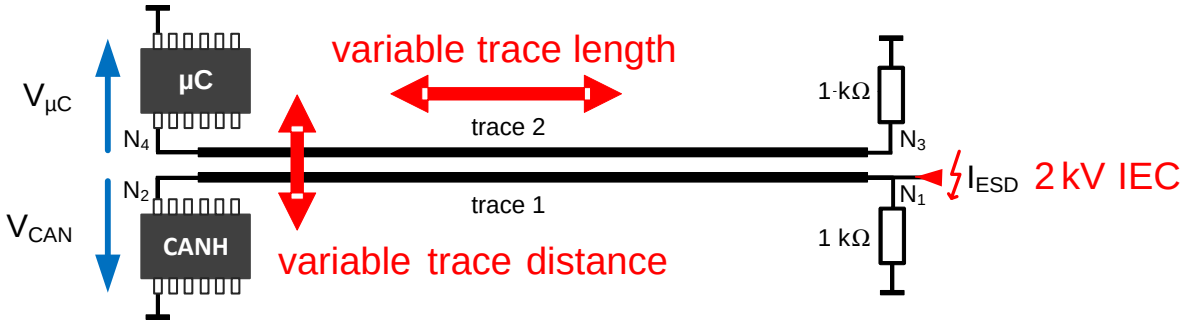

Figure 228: Simulation setup with variable trace length and trace distance for ICs

Similar effects as for resistors can be observed. The energy at node N2 is nearly stable for variable trace length and distance. Because of the I-V characteristic of the CANH pin about 40 % of the energy are calculated in comparison to Figure 226. Amplitudes at the µC pin are even lower. For the shortest trace distance and 200 mm trace length about 3,5 nJ are obtained.

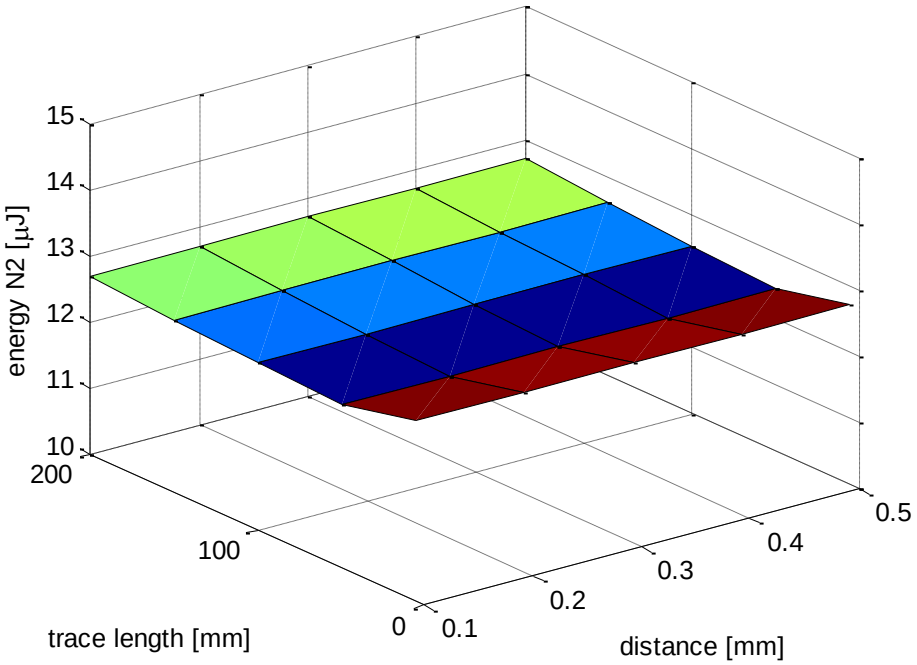

Figure 229: Energy of simulated IEC 2 kV discharge at node N2 at CANH-pin

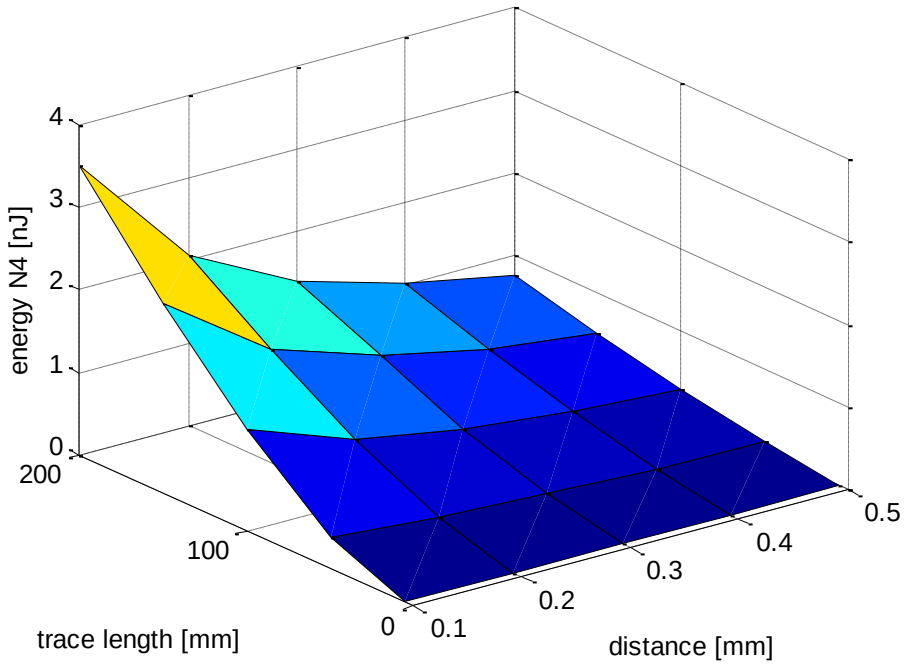

Figure 230: Energy of simulated IEC 2 kV discharge at node N4 at µC Data-pin

5.8 Critical case simulation

Based on the simulation results in previous sections setups with some trace configurations with strong coupling properties could be found. For the parallel trace configuration coupling becomes very large if the following values are chosen:

- narrow gap between the conductors (0,1 mm)
- conductor length (10 cm)
- distance from GND plane (1 mm)
- conductor width (1 mm)

With TXLINE impedances were calculated to Z_{even} = 95,08 Ω and Z_{odd} = 38,73 Ω. Three critical configurations were simulated using above parameters.

5.8.1 10 nF connected to trace 2

High current and voltage peak amplitudes can be obtained if a 10 nF capacitor is connected to node N3 at transmission line 2 according to Figure 231.

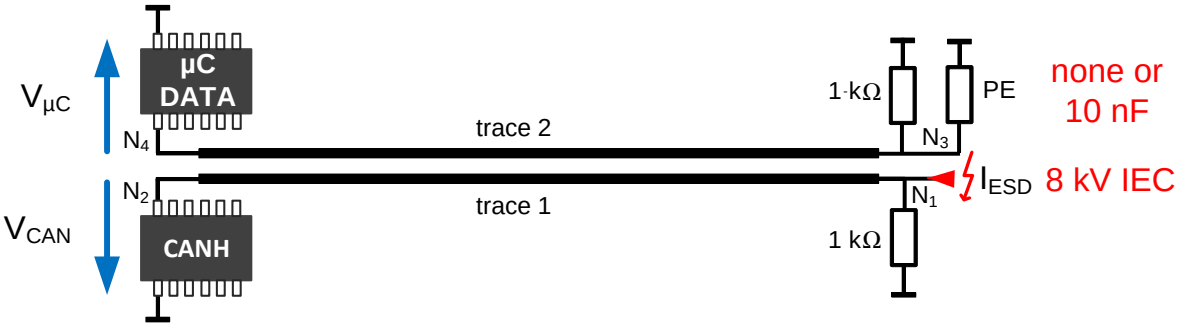

Figure 231: Simulation setup with protection element at node N3

In Table 40 the simulated quantities are compared for a 10 nF capacitor at node N3 and without ESD protection for 8 kV IEC charging voltage. Significant differences between peak voltages and currents can be obtained. Destruction is simulated for 1 kV and 2 kV HBM scaled µC models and for the 1 kV HBM scaled LIN model.

Termination	V_{charge} [kV]	V_{max} [V]	I_{max} [A]	E [nJ]	$E/E_{no\ protection}$
No ESD protection	8	4,00	0,81	5,84	1
Capacitor 10 nF	8	30,44	14,77	**1202**	205.82

Table 40: Simulated quantities at µC DATA pin at node N4 and 10 nF connected to node N3

5.8.2 10 nF connected to trace 2 and 220 pF at IC pin at trace 1

For some applications capacitors are connected to global IC pins. In Figure 232 220 pF were considered and current and voltage shapes were simulated at IC pins.

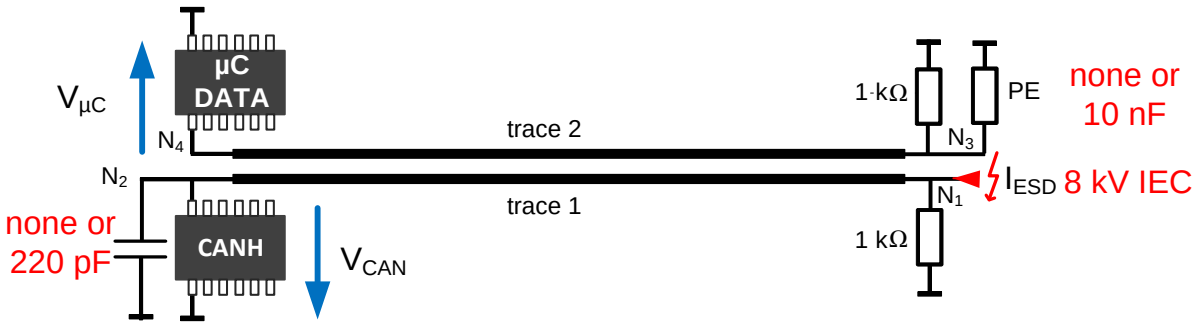

Figure 232: Simulation setup with 220 pF connected to node N2

According to Table 41 peak amplitudes and the energy are higher than without 220 pF capacitor. The voltage and current waveforms at CANH pin and µC pin are compared in Figure 233 to Figure 236 for the cases that only 10 nF is connected or 10 nF and 220 pF are connected to node N2. With 220 pF connected the peak current on trace 1 is higher and coupling may be stronger although less voltage amplitude is obtained at the CANH pin. At the time of discharge at node N1 the termination of the trace is not seen by the traveling wave. Simulated first peak voltage waveforms at node N1 are similar for the two described configurations.

Termination	V_{charge} [kV]	V_{max} [V]	I_{max} [A]	E [nJ]	$E/E_{no\ protection}$
No ESD protection	8	4,00	0,81	5,84	1
Capacitor 10 nF	8	30,44	14,77	**1202**	205.82
Capacitor 10 nF and 220pF	8	36.94	15,78	**1246**	213.82

Table 41: Simulated quantities at µC DATA pin at node N4 for 10 nF at N3 and 220 pF at N2

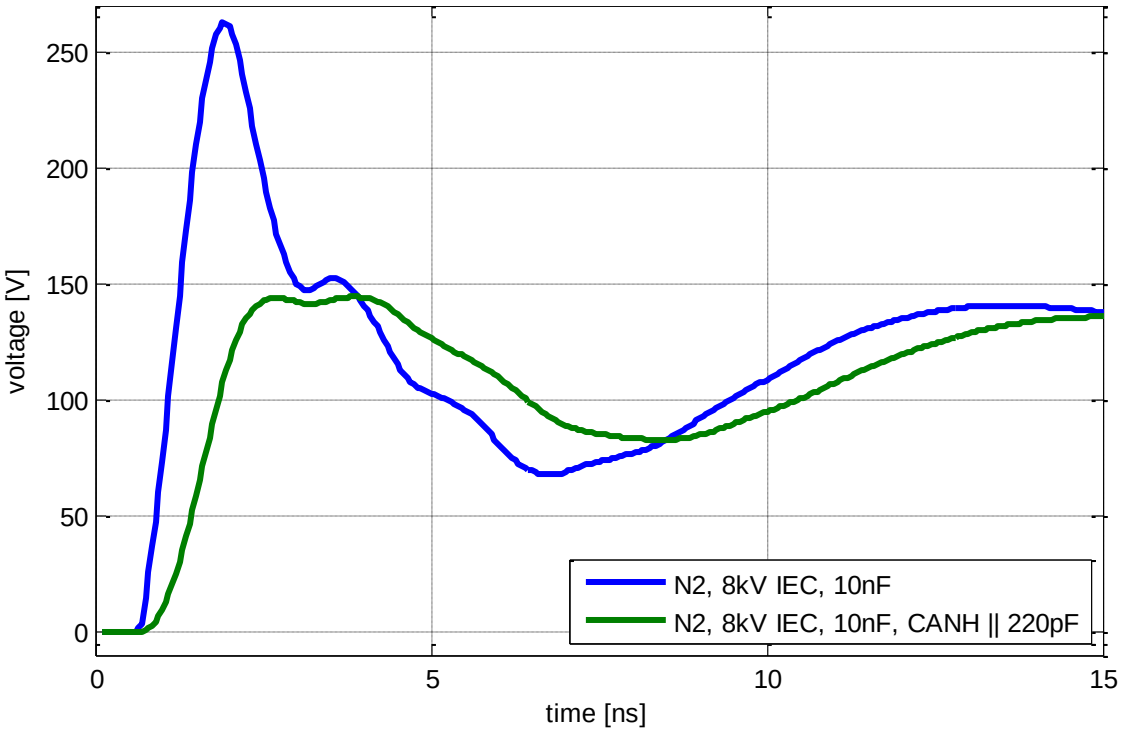

Figure 233: Comparison of simulated voltage shapes if 220 pF are connected to IC pin

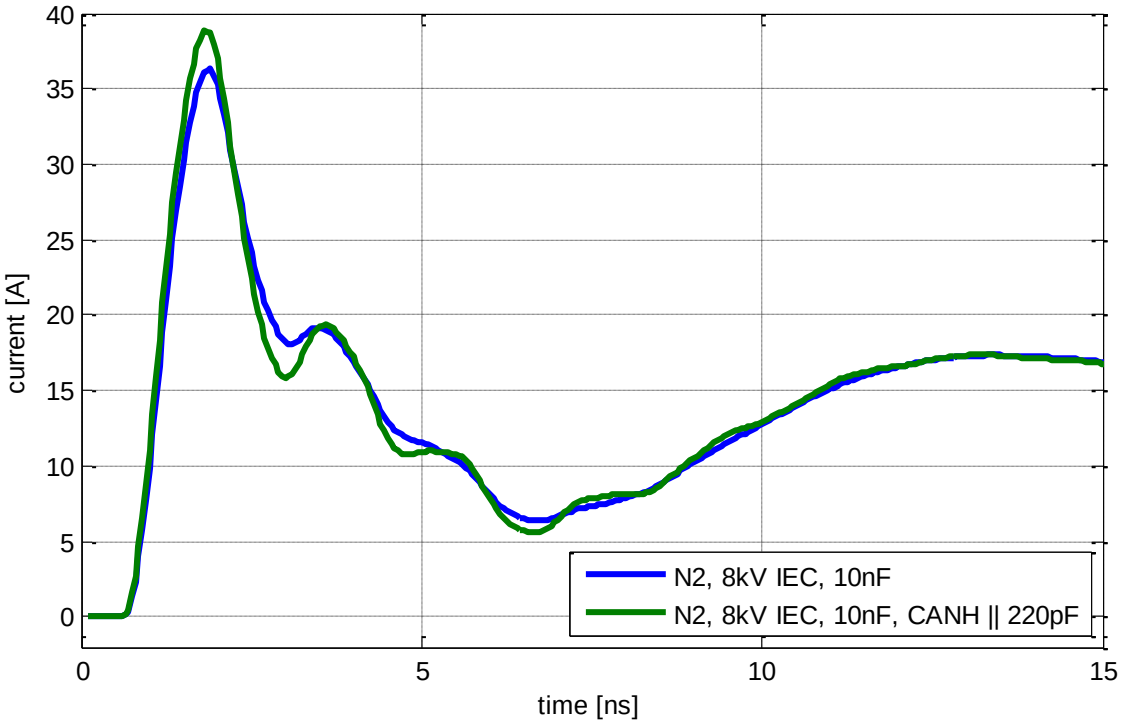

Figure 234: Comparison of simulated current shapes if 220 pF are connected to IC pin

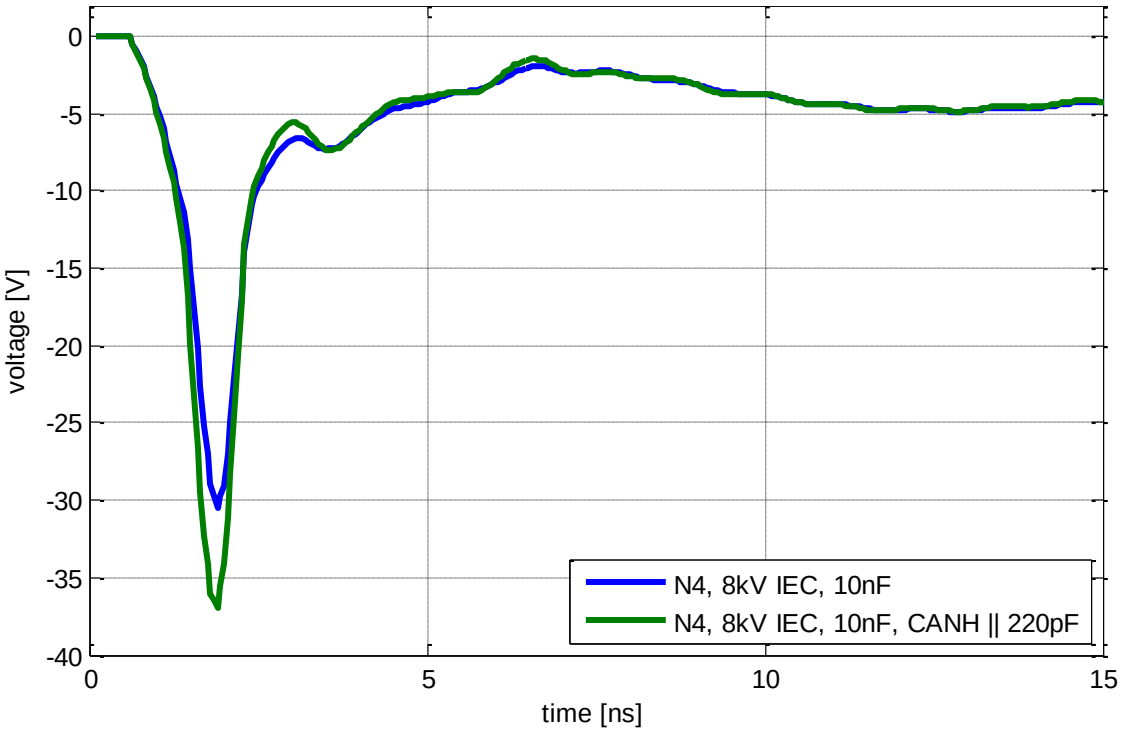

Figure 235: Comparison of simulated voltage shapes at µC pin if 220 pF are connected to N2

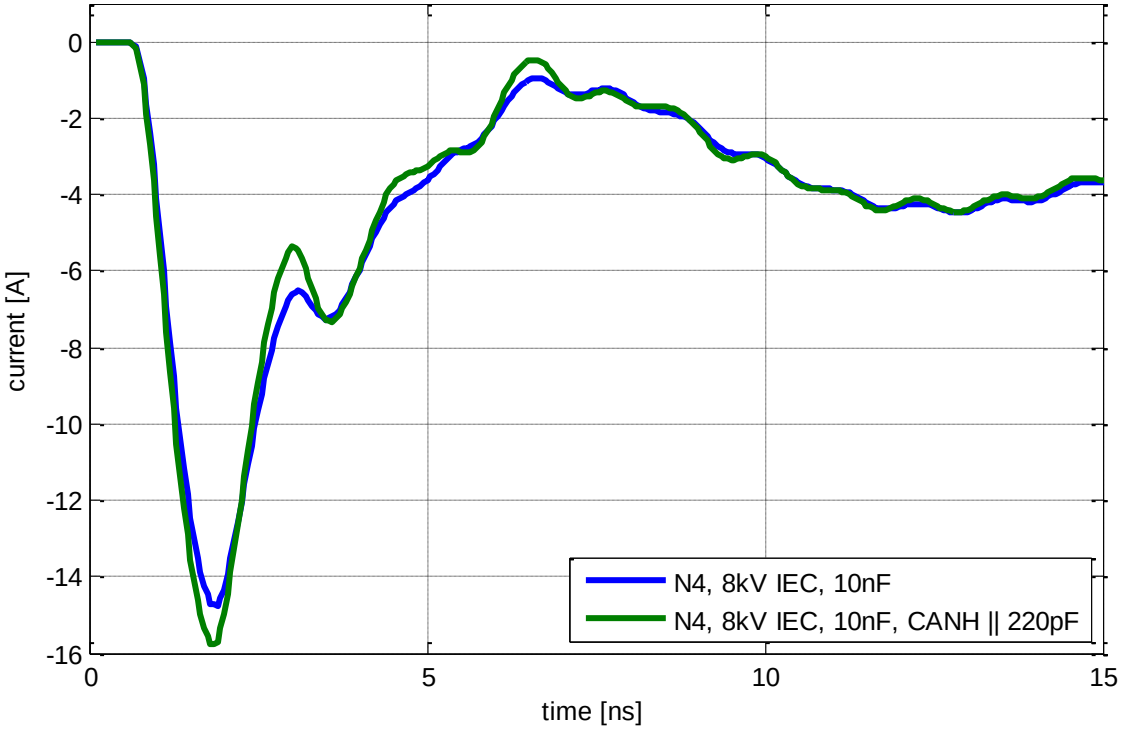

Figure 236: Comparison of simulated current shapes at µC pin if 220 pF are connected to N2

5.8.3 **Changed IC position**

In this section the setup shown in Figure 237 is simulated where the positions of the µC DATA pin and the protection element at the victim trace were interchanged. The difference between near-end and far-end cross-talk should be investigated.

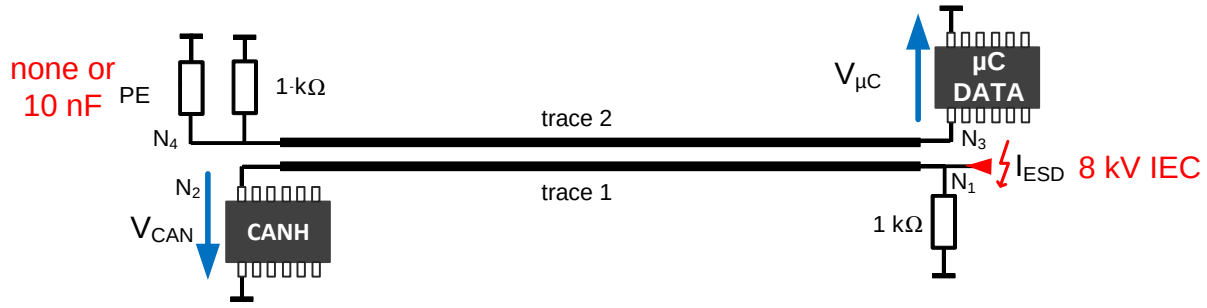

Figure 237: Simulation setup with protection element and changed IC position

Table 42 shows that the coupled energy without 10 nF capacitor connected is already high and reaches over 300 nJ which is close to the critical energy level of 350 nJ. If 10 nF are connected to node N4 even more energy is obtained at the µC pin although maximum amplitudes are less. Configurations described before can be considered to be more critical. But there might be even more critical configurations with different PCB geometries possible.

Termination	V_{charge} [kV]	V_{max} [V]	I_{max} [A]	E [nJ]	$E/E_{no\ protection}$
No ESD protection	8	22,07	13,63	304,82	1
Capacitor 10 nF	8	17,03	10,35	**1098**	3.61

Table 42: Simulated quantities at µC DATA pin at node N3

5.9 Impact of PCB traces and trace length on IC ESD robustness

The impact of a single transmission line on the IC ESD robustness is analyzed. In the setup shown in Figure 238 the LIN TxD IC model was connected to a trace with typical impedance of 83 Ω. The IEC ESD generator is discharged at node N1 or N2. Charging voltage is increased until IC failure can be simulated.

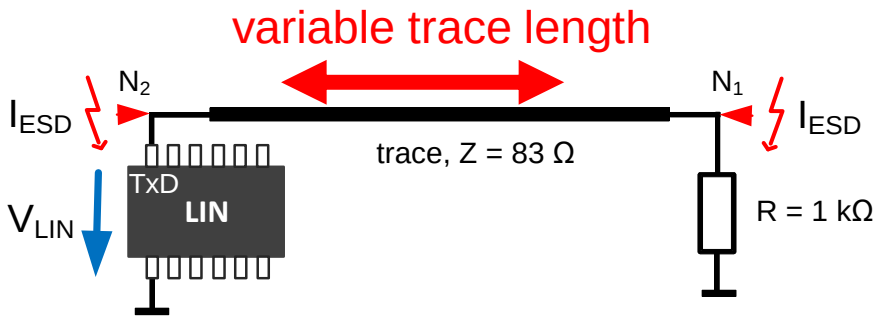

Figure 238: Simulation setup for discharges via LIN TxD pin at different positions N1 or N2

In Figure 239 the critical charging voltage is shown for variable trace length. The curves for discharges at N1 or N2 start at the same point for trace length of 0 mm. For 200 mm trace length only 100 V less charging voltage can be simulated, which is only about 3 %. Critical charging voltages are similar if the ESD generator is discharged via a trace or directly into an IC pin. No effect of transmission line can be observed in simulation if the ESD generator is discharged directly at the IC pin.

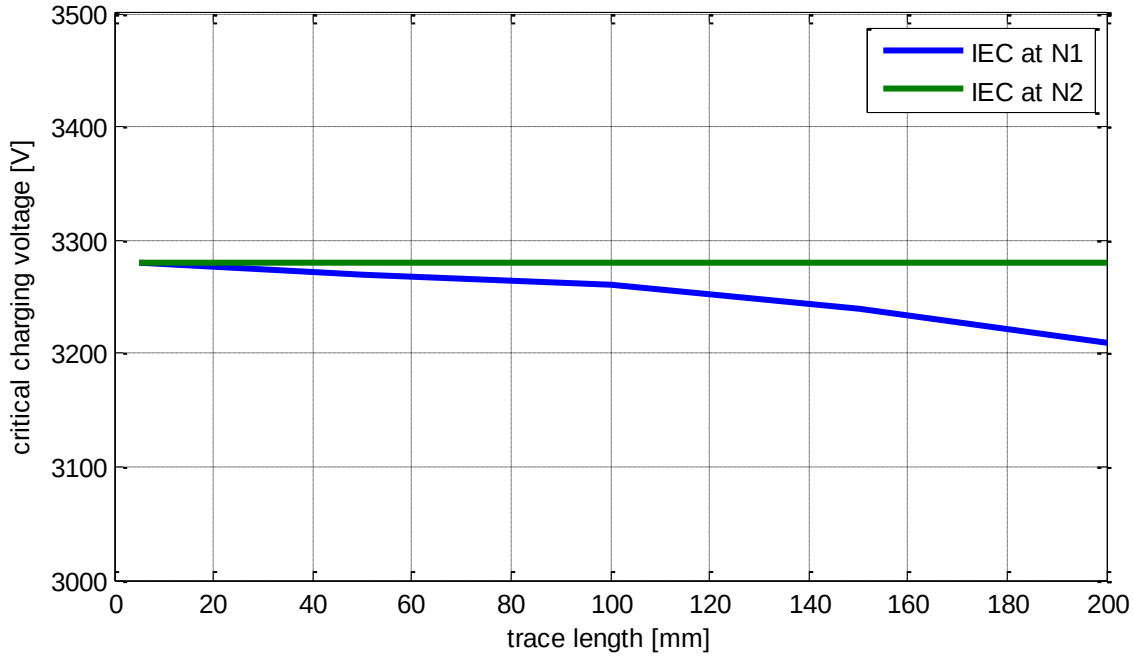

Figure 239: Simulated failure level for variable trace length

6 Design rules

In this section rules are proposed for reduced ESD cross-talk effects. No critical amplitudes and energies were observed for designs where ESD protection devices were placed on the conductor, where the ESD pulse is injected. ESD coupling effects increase if the conductor disturbed by cross-talk is terminated with low impedances for high frequencies. In Figure 240 a PCB of an automotive electronic control unit is shown. Global pins attached directly to the connector often are protected by capacitors close to the connector. Local PCB traces should have no capacitor and should be placed far away from traces connected to global pins.

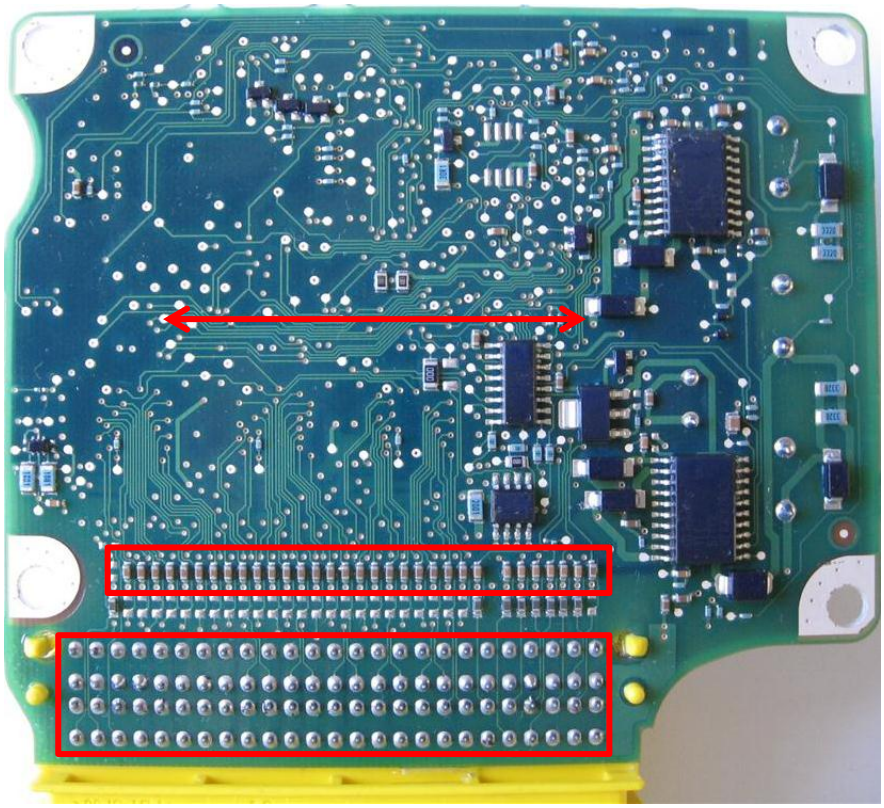

Figure 240: Automotive ECU

Some transmission lines are routed in parallel over a long distance. Optimal radiation of a transmission line is obtained at λ/2 resonance frequency. Assuming a propagation velocity of $2 \cdot 10^8$m/s the λ/4 wavelength at a frequency of 500 MHz is 10 cm. In many configurations propagation velocity is slower (15 cm/ns for ε_r=4). The critical frequencies are defined by minimum expected rise times of the ESD events. 5 up to 10 cm can be seen as critical lengths. Traces with a length of more than 5 cm should be checked carefully.

ESD cross-talk can be reduced considering some design rules for PCB traces. Some typical design parameters for a stripline configurations are shown in Figure 241.

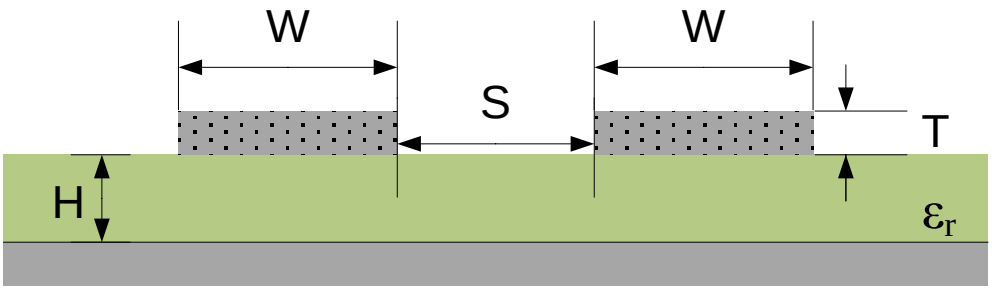

Figure 241: Basic parameters to calculate MTL impedances

Typical parameters for automotive PCBs can be:

W ≈ 0,254 mm

S ≈ 0,254 mm

H ≈ 0,5 mm

ε_r ≈ 4,2 mm

Even and odd impedances for a common automotive design can be calculated:

Z_{odd} = 68 Ω

Z_{even} = 116 Ω

Simulation results of an 8 kV IEC generator discharge and critical configuration with 10 nF connected to the conductor affected by cross-talk are given in Table 43. Typical PCB parameters were used. The conductor length is 5 cm. The CANH IC pin is connected to the conductor where the ESD pulse is injected and the µC DATA pin to the second parallel conductor. Maximum calculated energy reaches about 250 nJ. This energy level can be close to the critical value for 1 kV HBM scaled models. High peak amplitudes of about 9 V and 9 A can be obtained.

Load	**V_{charge} [kV]**	**V_{max} [V]**	**I_{max} [A]**	**E [nJ]**
No ESD protection	8	3,14	0,12	1,4
Capacitor 10nF	8	8,93	8,90	247

Table 43: Simulated quantities at µC DATA pin and safe parameters with 10 nF at trace 2

In Table 44 and Table 45 results are shown if an additional 10 nF capacitor is connected to conductor 1 where the ESD pulse is injected. For this topology only about 1 V and 170 mA were simulated at the µC pin if the IEC ESD generator is discharged with 8 kV charging voltage.

Load	V_{charge} [kV]	V_{max} [V]	I_{max} [A]	E [µJ]
No ESD protection	8	208,88	27,76	115,7
Capacitor 10nF	8	65,98	6,16	52,11

Table 44: Simulated quantities at CANH pin with 10 nF at trace 1 and 2

Load	V_{charge} [kV]	V_{max} [V]	I_{max} [A]	E [nJ]
No ESD protection	8	2,37	0,06	0,16
Capacitor 10nF	8	1,11	0,17	3,3

Table 45: Simulated quantities at µC DATA pin with 10 nF at trace 1 and 2

A parameter set for PCB traces that will probably cause no problems can be within the following limits:

$W \leq 0,5$ mm

$S \geq 0,2$ mm

$H \leq 0,5$ mm

$\varepsilon_r \leq 4,5$

For most designs the trace thickness T has negligible impact on coupling. The influence of the length of PCB trace is discussed above, it does not have any impact on the common mode and differential mode impedance, but for typical PCB dimensions it can be found that the longer a set of traces is, the more critical coupling might be.

Design rules for cross-talk can be formulated as following:

- Narrow distance (< 0,2 mm) between conductors should be avoided
- Conductor length should be as short as possible
- Distance from GND plane should be low (multi-layer is better than double layer)
- Conductor width should be small (< 0,5 mm)
- Low impedance terminations at victim trace should be avoided (protection elements!)

7 Summary

Possible IC destructions due to on-PCB-cross-talk between trace structures were investigated. IC ESD robustness was assumed to be 1 kV HBM.

A demonstrator PCB and two PCBs for IC characterization were designed and manufactured. Simulation models for all needed components were developed. ESD protection elements and pins of three different automotive ICs were characterized with a TLP measurement setup in time domain and with a network analyzer in frequency domain. Electrical models of all elements were created. It could be found for the analyzed IC pins that failure seems to be of thermal nature, thus thermal failure models of the ICs were implemented for simulation of the ESD robustness. After verification of the models created from measurements the thermal capacitance and resistance is scaled so that IC destruction energy levels change. Failure models with 2 kV and 1 kV HBM ESD robustness were designed.

In the scaled models only the thermal domain was changed. I-V characteristics of the original models were not modified. Scaled IC failure models could not be verified during investigations because ICs with lowered ESD robustness were not available.

Simulation techniques were the main tool to answer the project questions, due to this reason selected simulation results on system level were verified by measurement. Coupling between two parallel PCB traces (source and victim trace) was analyzed in frequency and in time domain. IEC generator and TLP discharges were simulated and measured using different load conditions. Cross-talk voltages and currents without and with connected ESD protection elements were simulated and measured.

The disturbance of ICs due to PCB cross-talk from ESD events can be described in terms of peak amplitudes and curve shapes of voltages and currents. Energy content can be calculated. These quantities mainly depend on the following parameters:

- Amplitude and curve shape of initial ESD pulse
- Geometrical properties of PCB traces
- Termination impedance of PCB traces
- Impedance of ESD source

Coupling between two PCB traces was simulated for a specified configuration with different resistances as loads and different pulse sources. It could be shown that the coupled peak voltages on parallel victim PCB traces are in the range of 30 % of the values over the source trace for high load resistances. For low impedances the coupled voltages are much lower. The energy levels coupled to parallel traces are much lower and below 1 % of the injected ESD energy. Energy and peak amplitudes reach maximum level on source trace if the load and the pulse source match the transmission line impedance. Most energy was simulated for a 50 Ω TLP discharge and R_{load} = 100 Ω. The transmission line impedance is about 80 Ω. If signals on source trace are reflected the coupled pulse energy increases for the same transmission line parameters.

Increasing charging voltage of testing devices causes a linear rise of current and voltage amplitudes on parallel conductors if resistors are used as loads. Pulse energy increase quadratic with the factor of increasing charge voltage. The electrical behavior of ICs is determined by a non-linear I-V characteristic. Peak amplitudes of voltage and current waveforms at the IC input depend on the breakdown voltage of the IC ESD protection circuit. Cross-talk peak amplitudes of 30 V and about 15 A were simulated for an 8 kV IEC discharge using a worst case setup. Due to nonlinear behavior energy levels do not follow the quadratic relation compared to the factor of charging voltage increase. A critical configuration for many termination cases is a capacitive loads connected to victim trace. This can cause high currents because of the low impedance for high frequencies.

Simulated coupled energies of ESD events are lower if transmission lines are connected to high impedance loads models. The lowest computed failure energy of scaled 1 kV HBM IC models was 350 nJ for the µC DATA pin. 2 kV HBM scaled models are destroyed for pulse energies higher than 820 nJ. Exceedance of the critical failure level of 350 nJ could be simulated for setups without ESD protection connected to source trace and e.g. a 10 nF capacitor connected to victim trace. Over 600 nJ could be obtained in case of an 8 kV IEC generator discharge.

Critical configurations could be figured out for setups where no ESD protection was connected to injection node of source trace. Far end needs to be terminated with a low impedance termination. When victim trace forms a low impedance loop coupled energy can be high. For setups with effective protection elements connected to source trace amplitudes of less than 4 V and 10 mA were simulated for 8 kV IEC discharges. Amplitudes and energies of loop induced pulses are not critical.

Cable discharges are not critical if rise times are comparable to IEC generator discharges. Measured energy of cross-talk signals from 50 Ω TLP with 400 V charging voltage was about 20 nJ. Peak voltage of less than 25 V and peak current less than 1 A. All termination elements were 50 Ω resistors. Energy and current peak amplitudes are even lower if high impedance IC inputs are connected.

All results are very sensitive to variations of the topology and configuration. In order to verify ESD robustness of a design individual simulations of a PCB configuration are necessary.

8 References

[1] Industry council on ESD Target Levels. White Paper 1: A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements.

[2] DKE Deutsche Kommission Elektrotechnik Elektronik Informationstechnik im DIN und VDE, AK 767.13.14_2010-0015. Positionspapier ESD WP1. 2010.

[3] JEDEC Solid State Technology Association. Reference number JESD22-A114F, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM). 2008.

[4] K. Esmark, H. Gossner, and W. Stadler. Advanced Simulation Methods for ESD Protection Development. Elsevier Ltd, Oxford, 2003. ISBN 0-08-044147-5.

[5] F. zur Nieden, B. Arndt, J. Edenhofer, S. Frei. Vergleich von ESD-System-Level Testmethoden für Packaging und Handling. ESD-Forum 2009. Berlin, 2009.

[6] F. zur Nieden, Y. Cao, B. Arndt, S. Frei. Vergleichbarkeit von ESD-Prüfungen auf IC- und Systemebene oder welchen Einfluss hat eine Reduzierung der IC-ESD-Festigkeit auf die Systemfestigkeit?. EMV-Düsseldorf. 2010.

[7] High Power Pulse Instruments GmbH. TLP/VF-TLP/HMM Test System TLP-3010C/3011C. Product Brief. Rev. 1.7. 2010

[8] Y. Cao, B. Arndt, F. zur Nieden, F. Kremer, M. Stecher, S. Frei. Charakterisierung und systematische Bewertung von externen ESD Schutzelementen. EMV-Düsseldorf. 2010.

[9] Y. Cao, W. Simbürger and D. Johnsson. Rise-Time Filter for Transmission-Line Pulse Measurement Systems. German Microwave Conference IEEE. 2009.

[10] K. Siebert, H. Günther, S. Frei, W. Mickisch. Modeling of Frequency Dependent Losses of Transmission Lines with VHDL-AMS in Time Domain. International Zurich EMC Symposium Zurich. Switzerland. 2009

[11] Paul, Clayton R. Analysis of Multiconductor Transmission Lines. New York John Wiley & Sons, Inc, 1994. ISBN 047102080X

[12] B. Arndt, F. Kremer, F. zur Nieden, Y. Cao, J. Edenhofer, S. Frei. Modellierung und Simulation von ESD-Schutzelementen mit VHDL-AMS. EMV-Düsseldorf. 2010.

[13] Keithley Instruments, Inc. 2400 Series SourceMeter. User´s Manual. Rev. J. 2007.

[14] D. C. Wunsch, R. R. Bell. Determination of Threshold Failure Levels of Semiconductor Diodes and Transistors due to Pulse Voltages. IEEE Transactions on Nuclear Science. 1968.

[15] H. Baumgärtner, R. Gärtner. Elektrostatische Entladungen (ESD). ISBN-13: 978-3835638037. Oldenbourg Verlag. 1997.

[16] http://web.awrcorp.com/. AWR Corporation. TX-Line™ Transmission Line Calculator. 2011